Figure 1: Conformal Polymer Layer(s) on Substrate/Conductors/Previous Layers
(Ground metallization over conformal coating is optional)

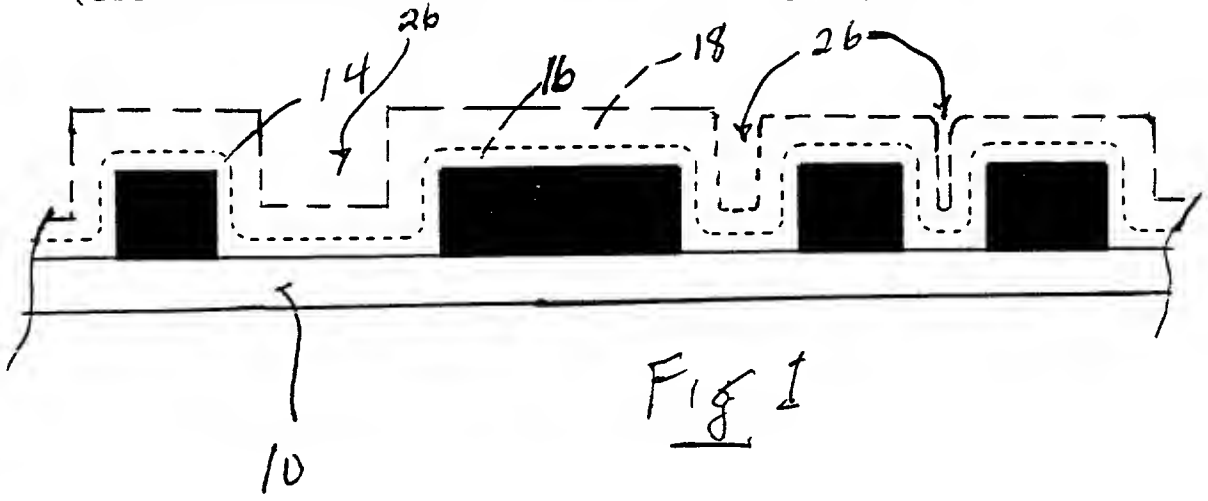


Fig 1

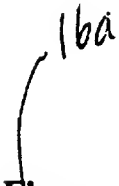


Figure : After deposition of gapfilling polymer and CMP
(Conformal polymer may now be deposited again for next layer)

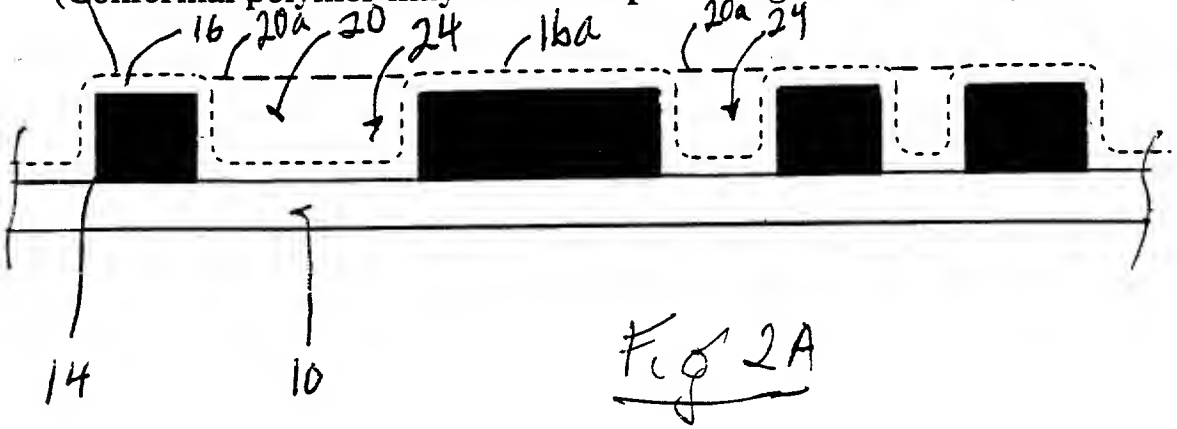


Fig 2A

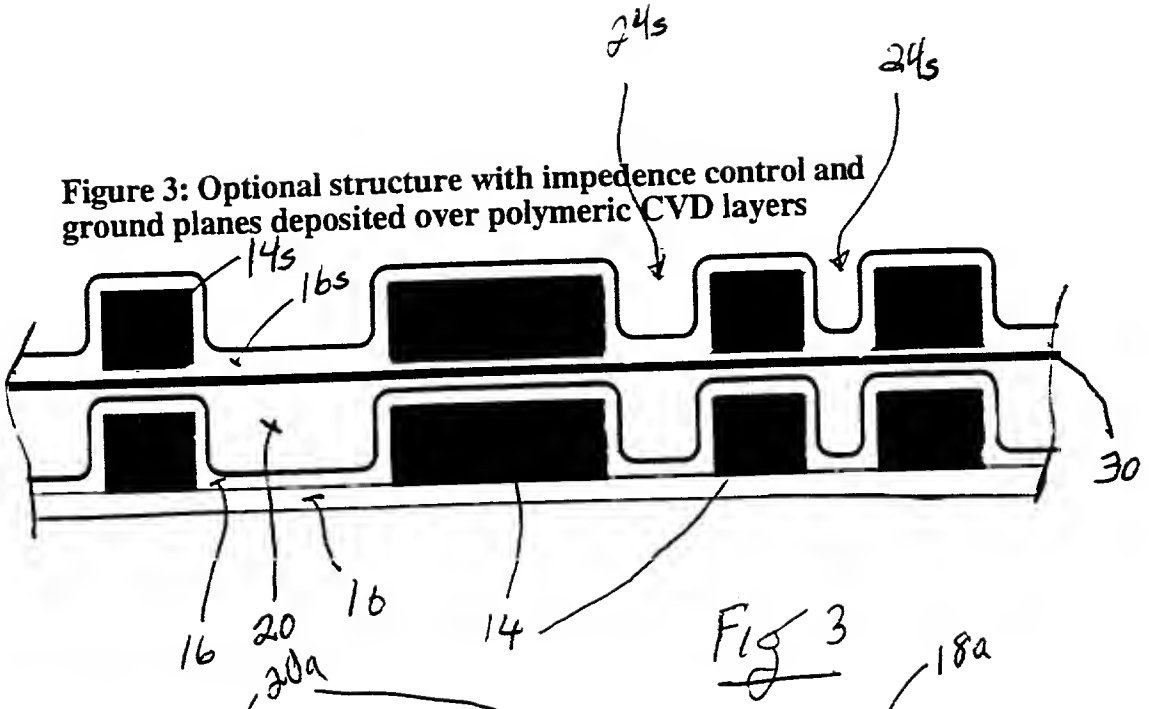


Figure 3: Optional structure with impedence control and ground planes deposited over polymeric CVD layers

Fig 3

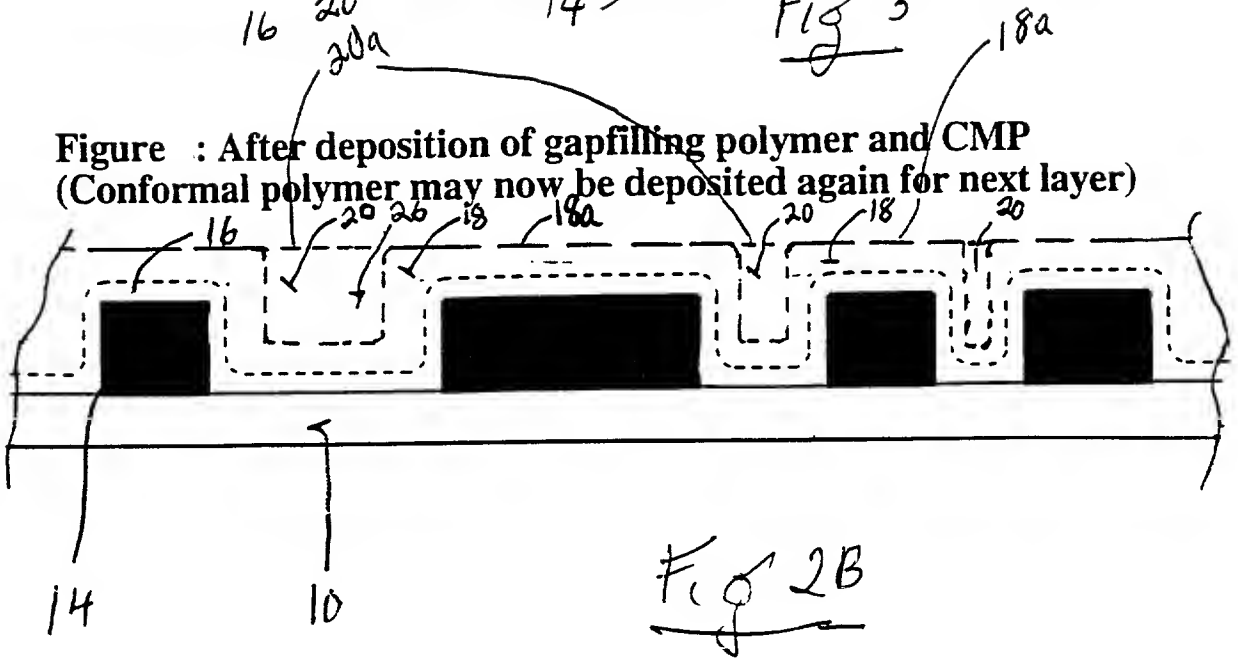


Figure : After deposition of gapfilling polymer and CMP (Conformal polymer may now be deposited again for next layer)

Fig 2B

Figure 1: a) Circuit on substrate with Conformal Polymer Layer(s) on Substrate/Conductors/Previous Layers.
b) Masking can be used to make polymer layer discontinuous from conductor to conductor.

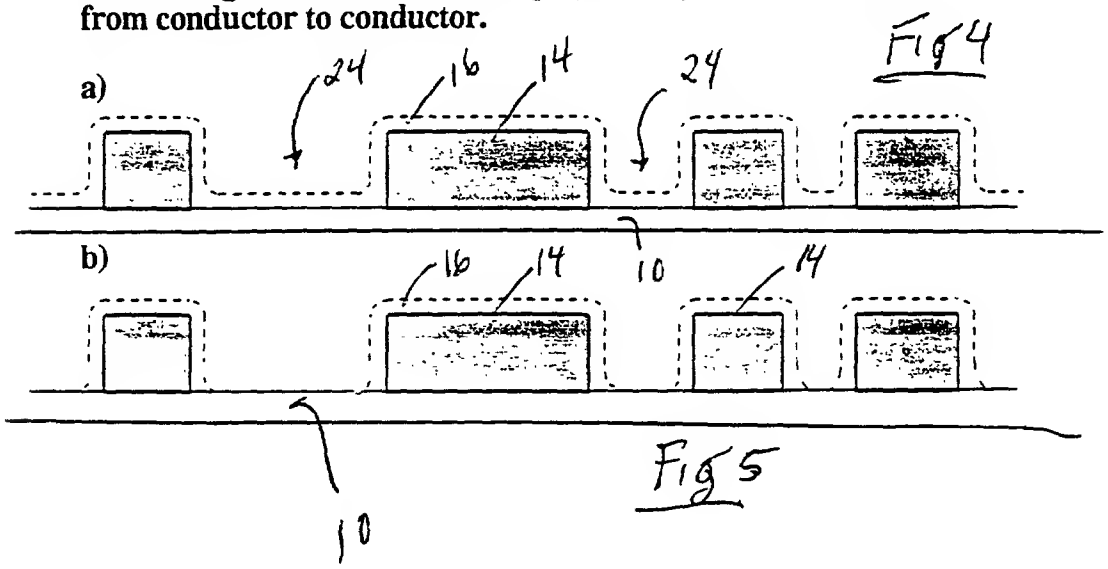


Figure 2: Organic or Inorganic gap filling layer is provided. This layer may be continuous or discontinuous (foam or full of voids/cracks. Previous conformal layer serves as adhesion promoter, and diffusion barrier.

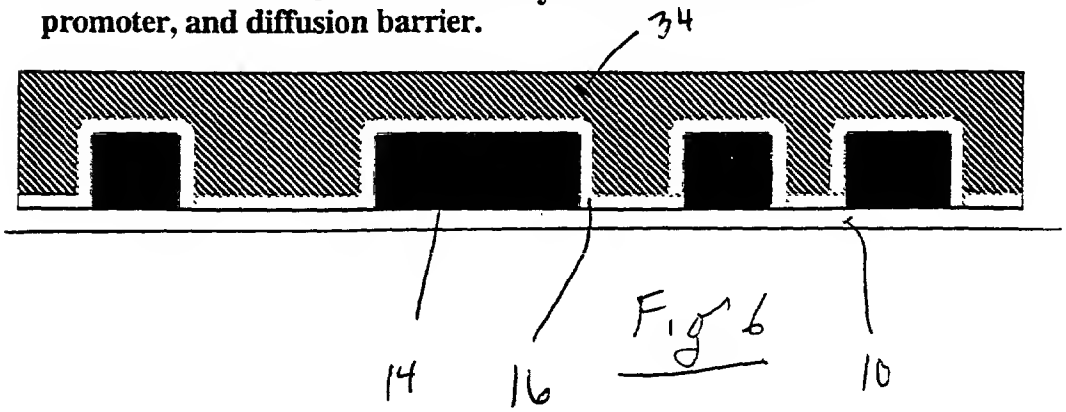


Fig 7

Figure 3: Planarizing Layer(s) to act as compliant sealant layers, facilitate CMP and further buildup

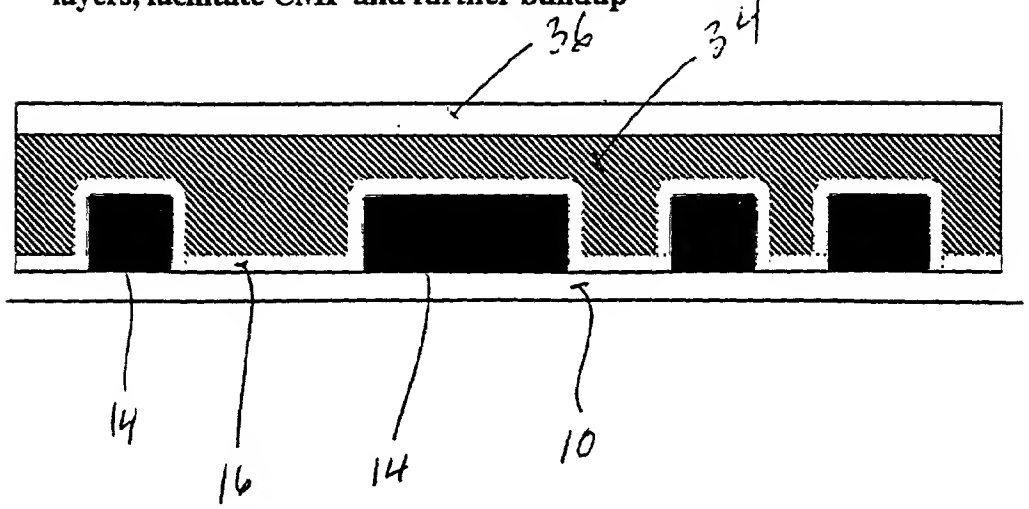


Fig 8

Figure 4:
Shown with subsequent build up of successive layer.

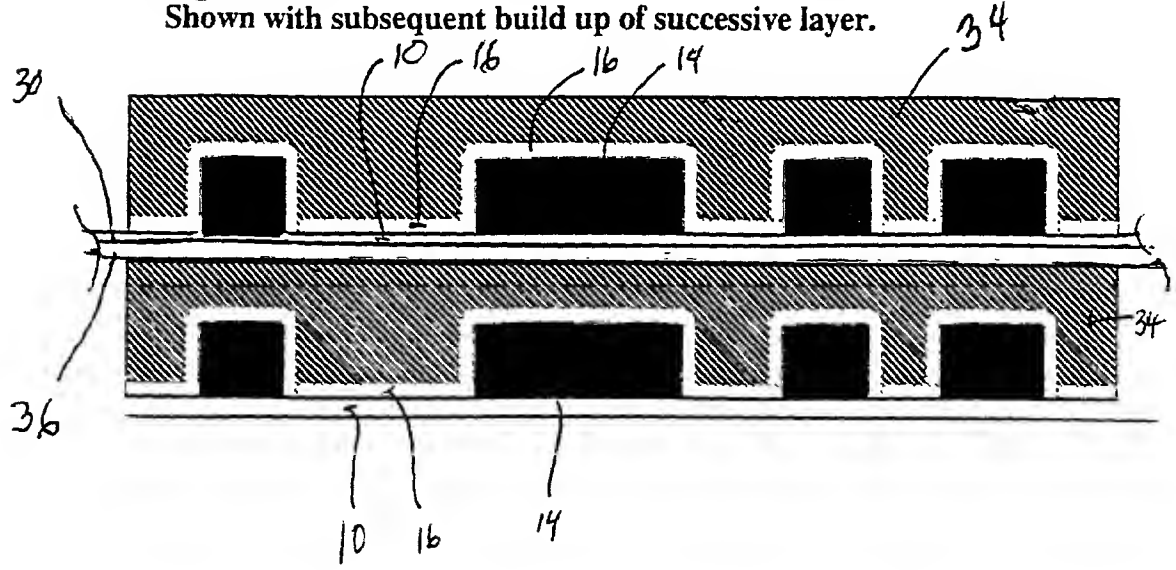
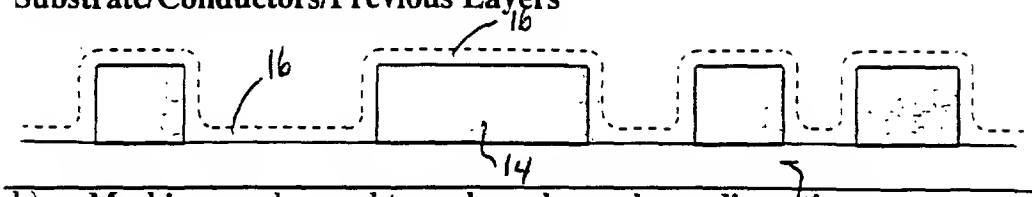


Fig 9

Figure 1: a) Conformal Polymer Layer(s) on Substrate/Conductors/Previous Layers



b) or Masking can be used to make polymer layer discontinuous from conductor to conductor.

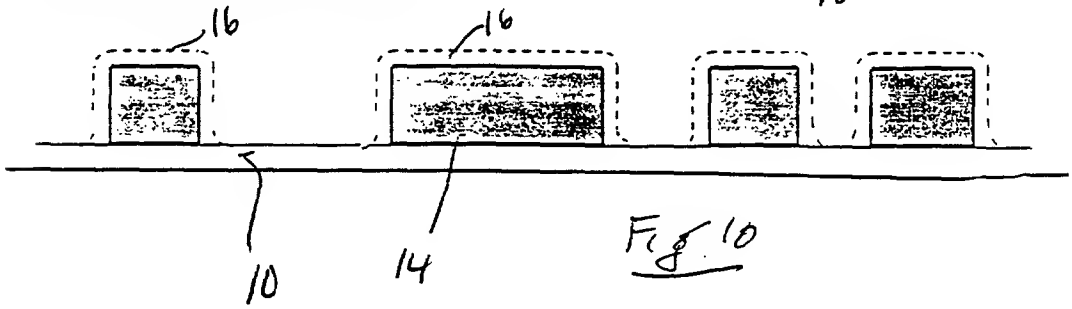


Fig 10

Figure 2: Application of Low Dielectric Constant Thermoplastic Particulates.

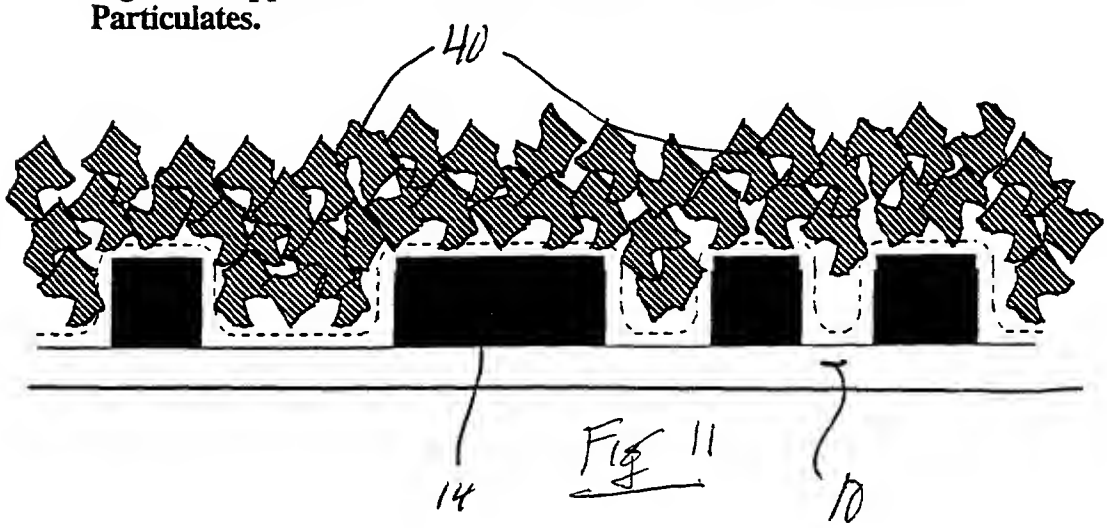


Fig 11

Figure 3: Following Thermal Treatment (e.g., autoclave or lamination). Possible Voids may be retained in thermoplastic region .

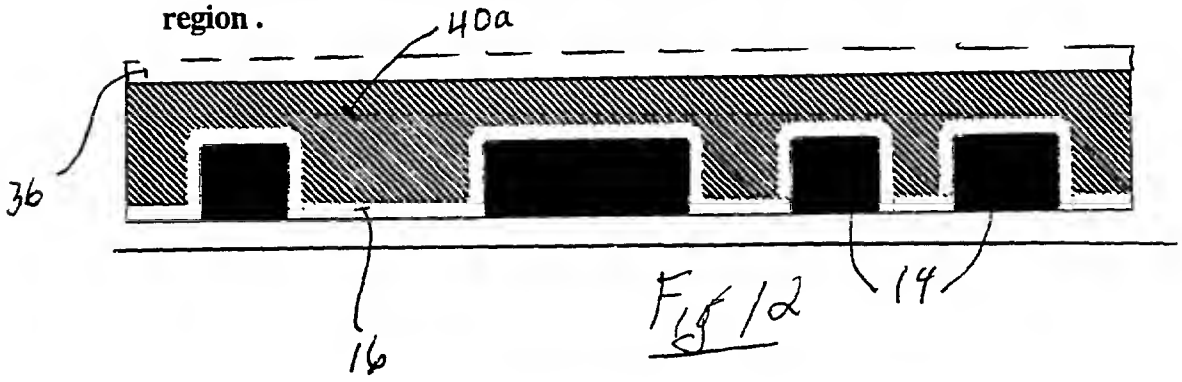


Fig 12

Figure 4: Following a planarization step, another conformal polymer layer is deposited upon which fuurther circuit buildup may take place. An optional ground layer may be deposited prior to second layer buildup for dimensional stability and/or electrical performance.

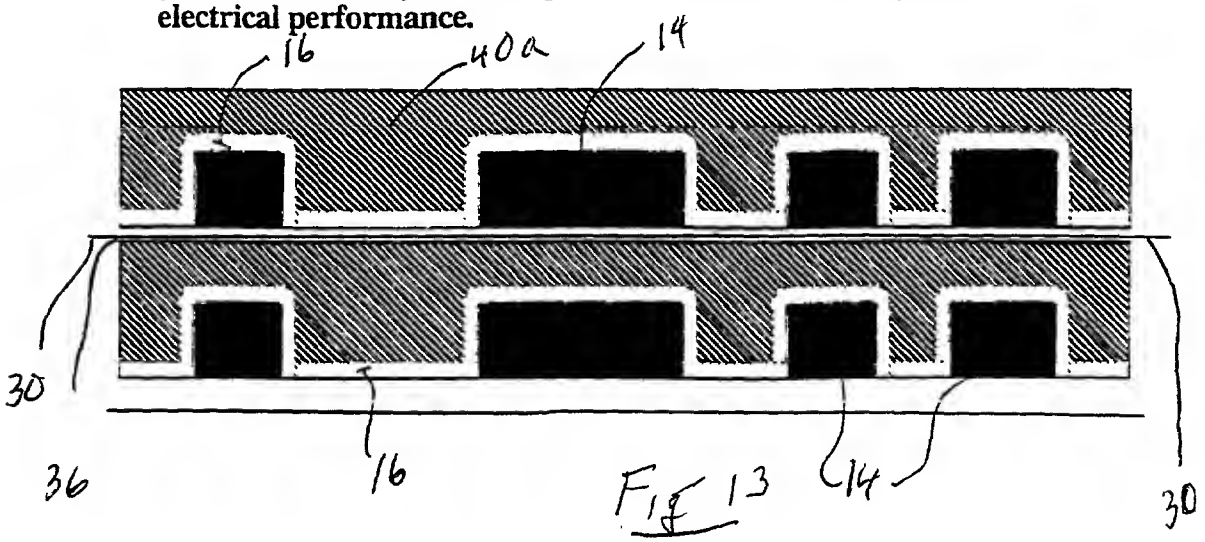
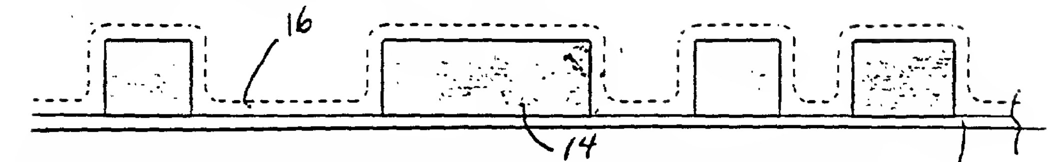


Fig 13

Fig 14

Figure 1: a) Conformal Polymer Layer(s) on Substrate/Conductors/Previous Layers



b) or Masking can be used to make polymer layer discontinuous from conductor to conductor.

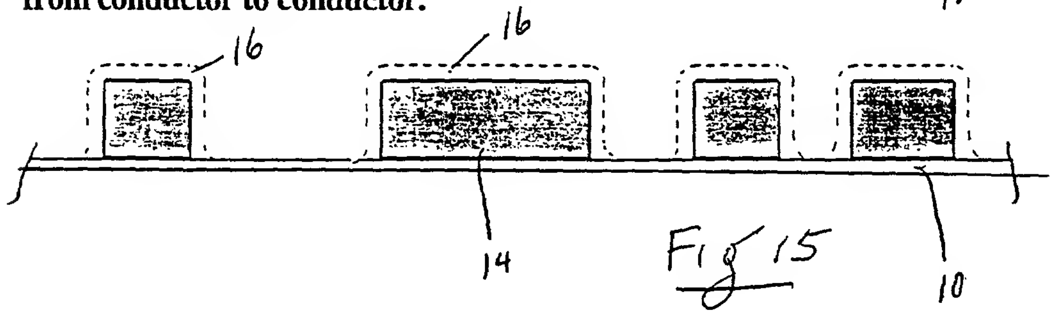


Fig 15

Figure 2: Application of Composite Low Dielectric Constant Polymer Particulates within another planarizing Low Dielectric Constant Polymer. Particulates may be co-sprayed with the fluid, pressed into fluid or the fluid may be spun on lightly compressed (and/or partially sintered) particulates. Alternatively the particulates may be precipitated out of solution. After Curing an additional CMP step may be performed.

Fig 16

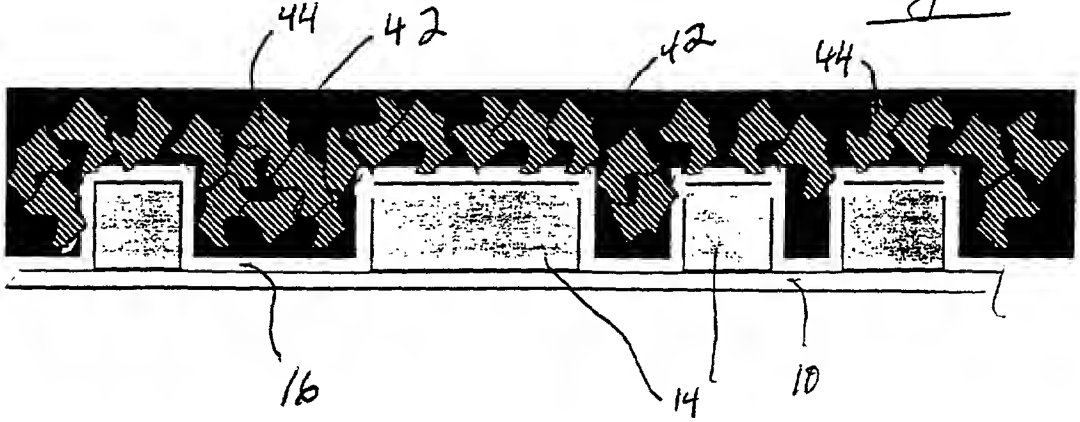


Figure 3: Another conformal polymer layer is optionally deposited upon which further circuit buildup may take place. An optional ground layer may be deposited prior to second layer buildup for dimensional stability and/or electrical performance.

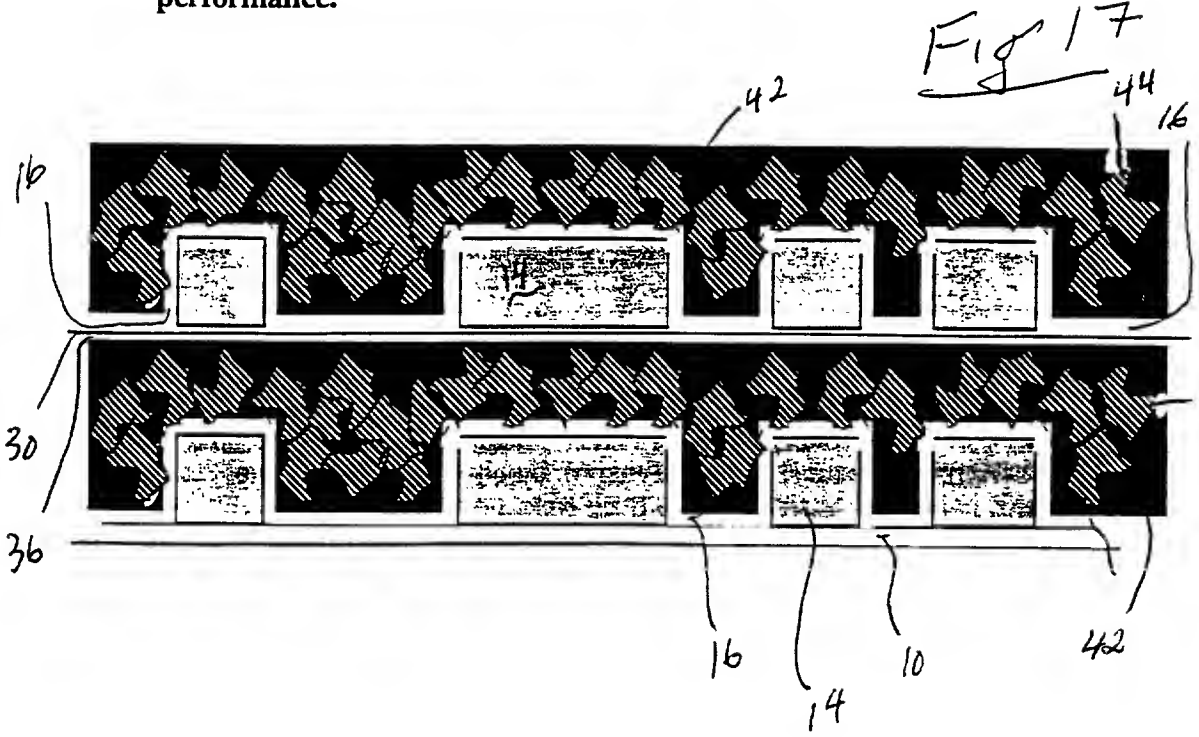
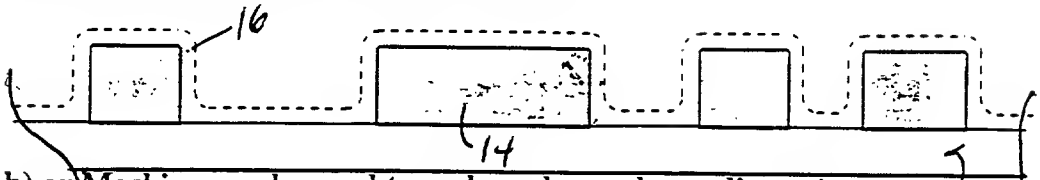


Figure 1: a) Conformal Polymer Layer(s) on Substrate/Conductors/Previous Layers

Fig 18



b) or Masking can be used to make polymer layer discontinuous from conductor to conductor.

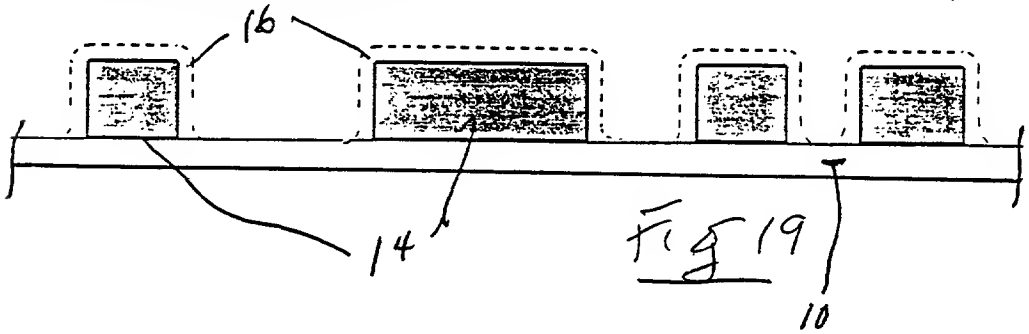


Fig 19

50

Figure 2: Thermoplastic Low Dielectric Constant Polymer Film is placed on top of circuitry.

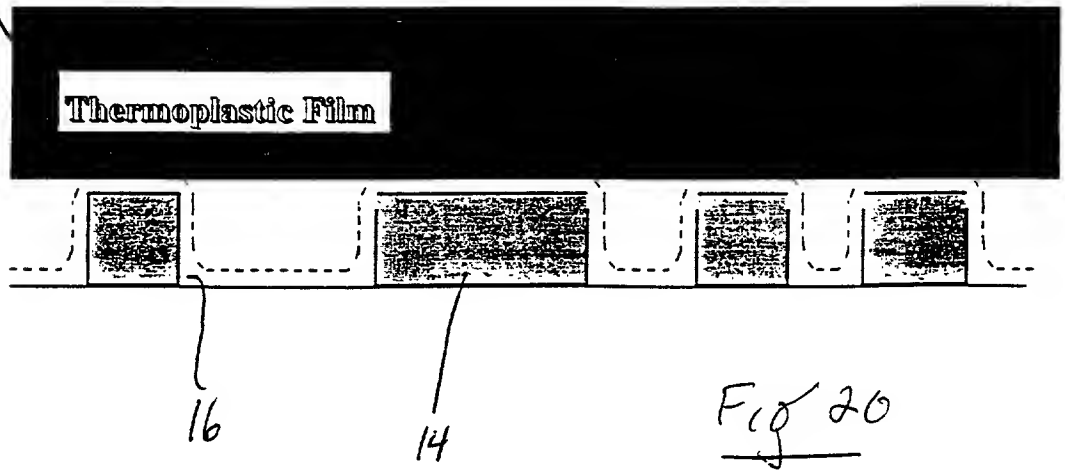


Fig 20

Figure 3:
Thermal Application of Thermoplastic Low Dielectric Constant Polymer Film. Film may be laminated or autoclaved. Another conformal polymer layer is optionally deposited upon which further circuit buildup may take place. Another option is to combine a planarizing layer deposited over the surface to facilitate CMP. An optional ground layer may be deposited prior to second layer buildup for dimensional stability and/or electrical performance.

Fig 21

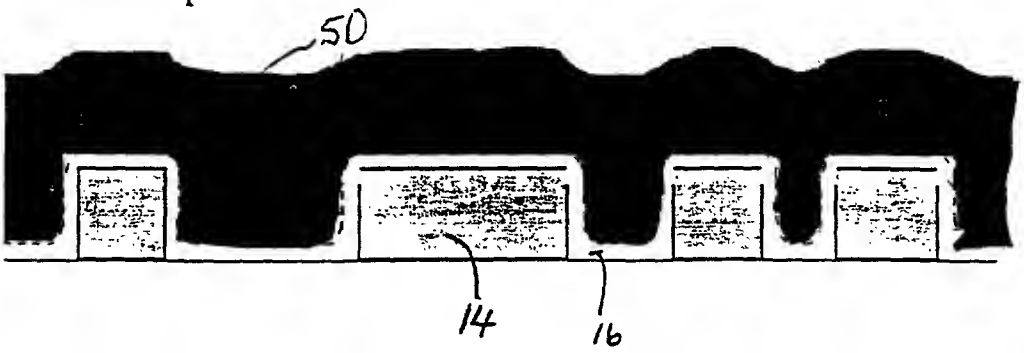
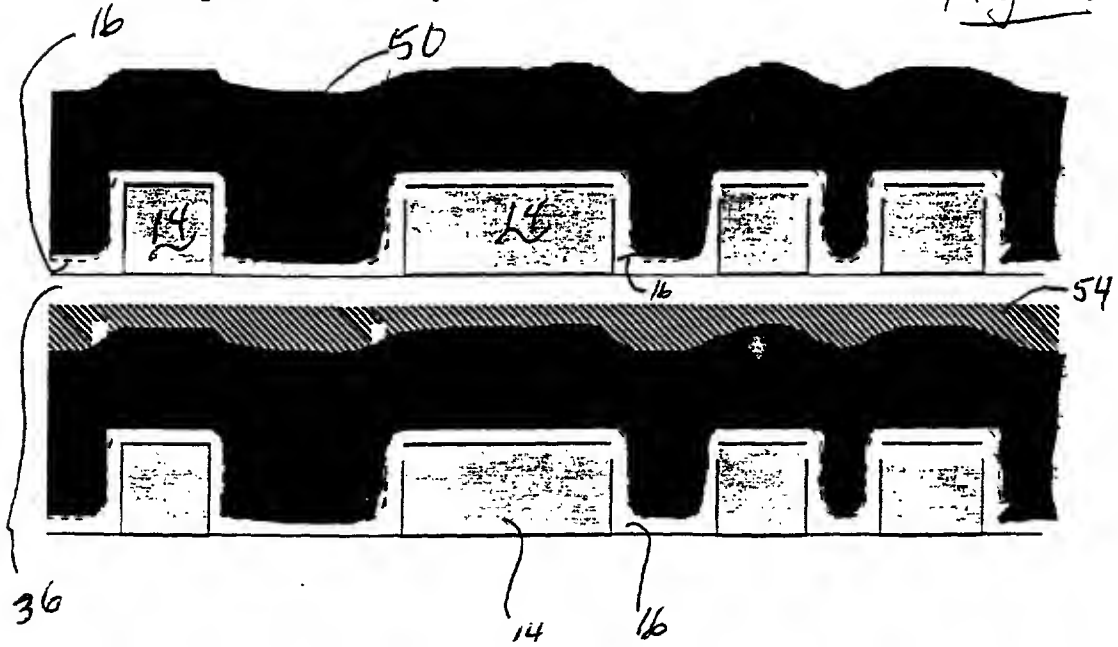


Figure 4:
Shown with the optional planarizing layer and subsequent build up of successive layer.

Fig 22



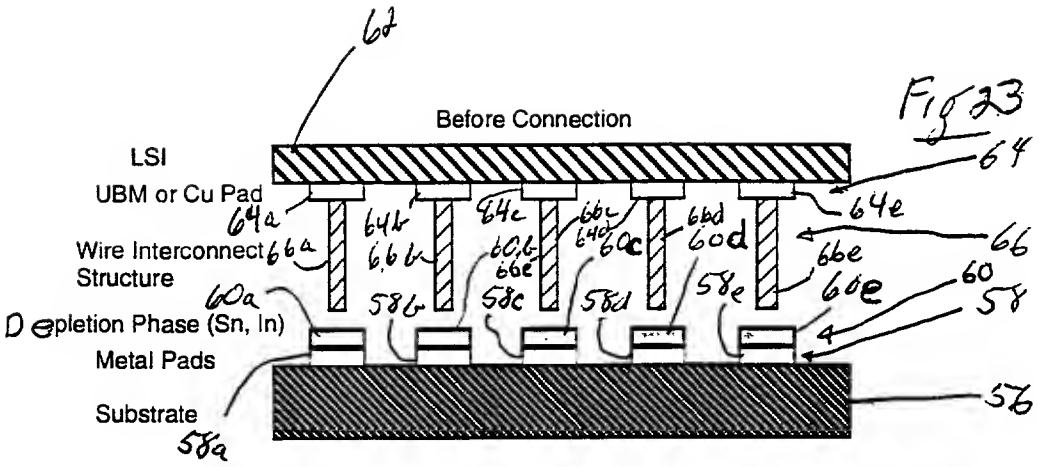


Fig 23

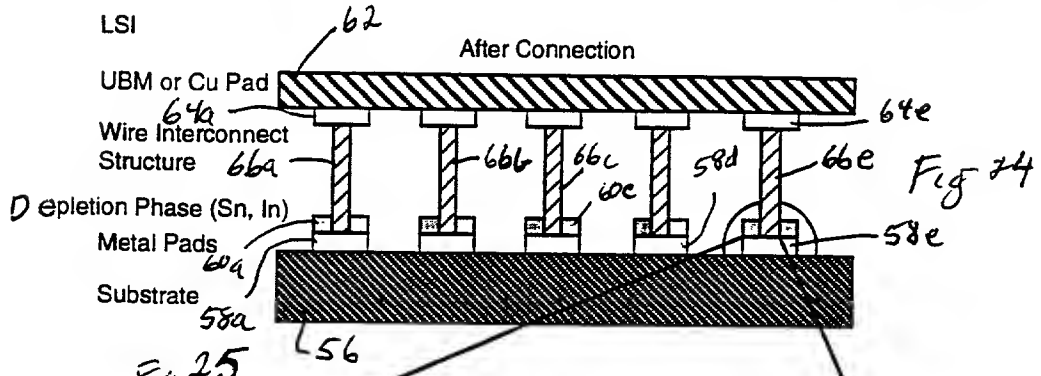


Fig 24

Fig 25

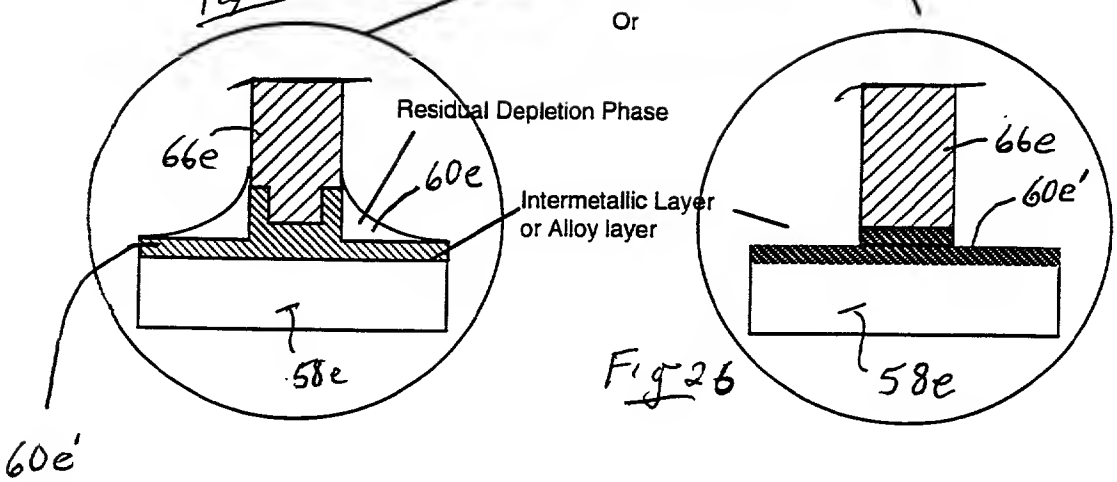


Fig 26

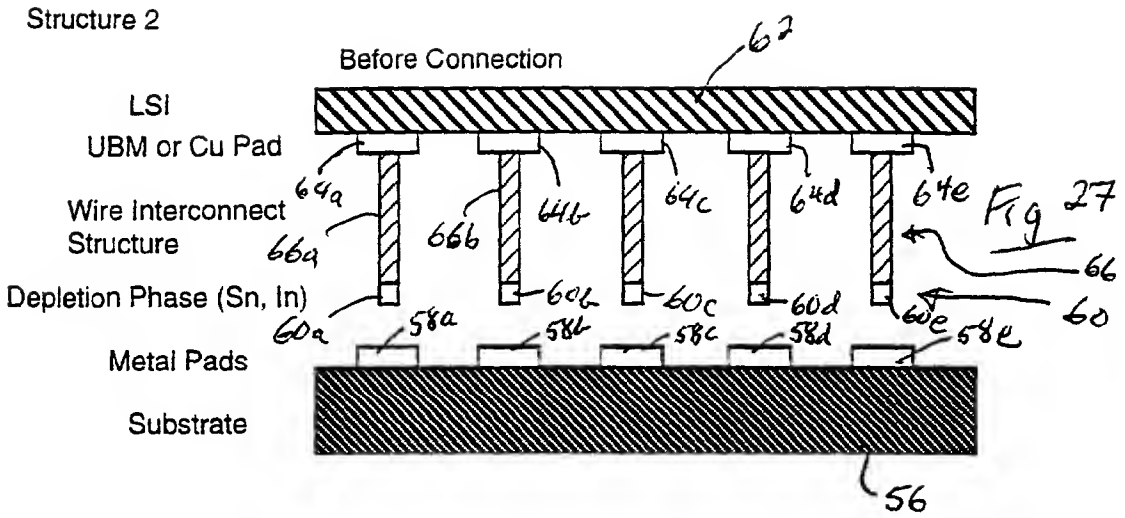


Fig 27

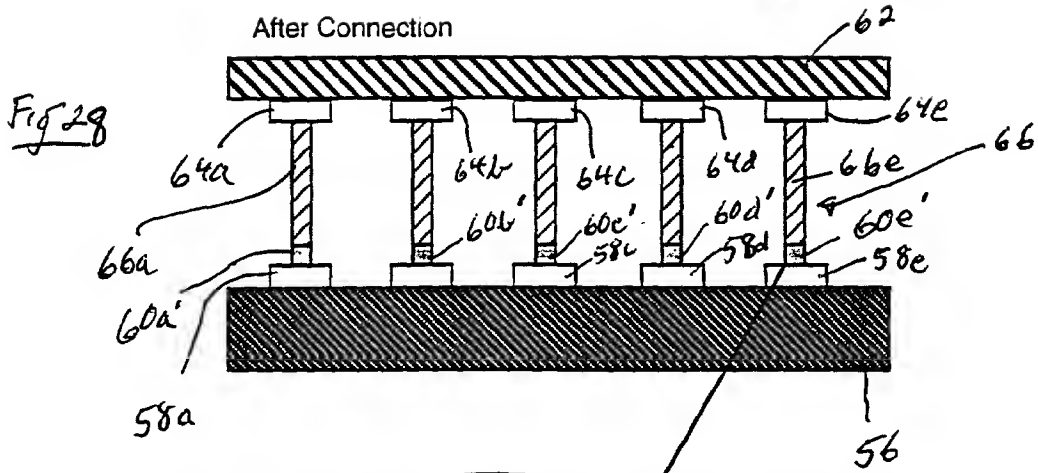


Fig 28

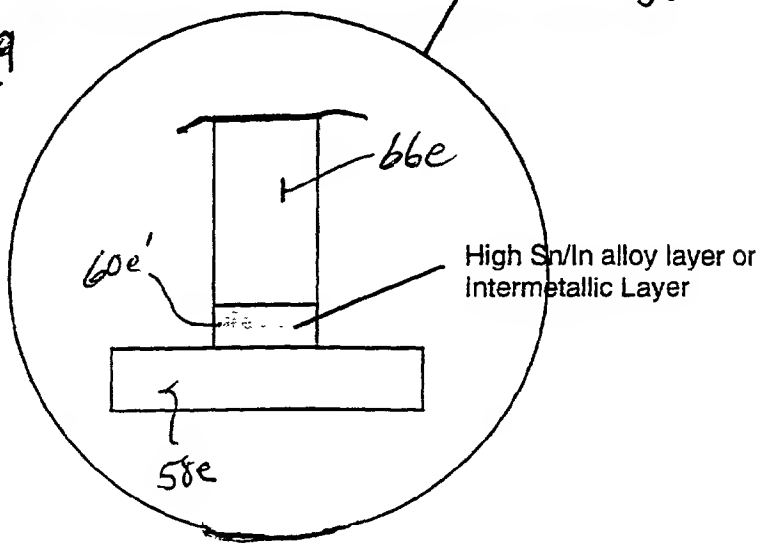


Fig 29

Structure 3

Fig 30

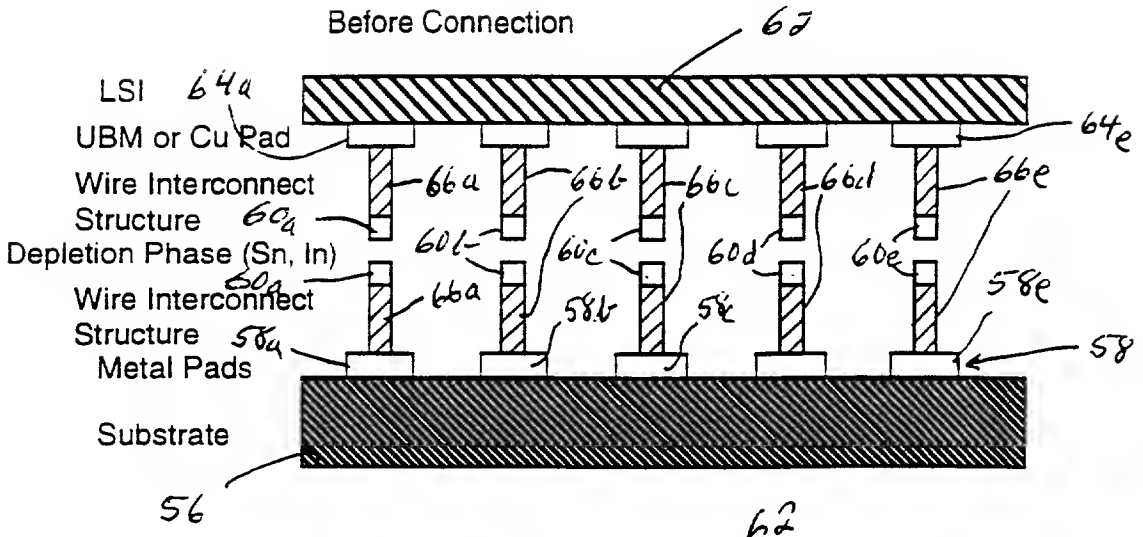


Fig 31

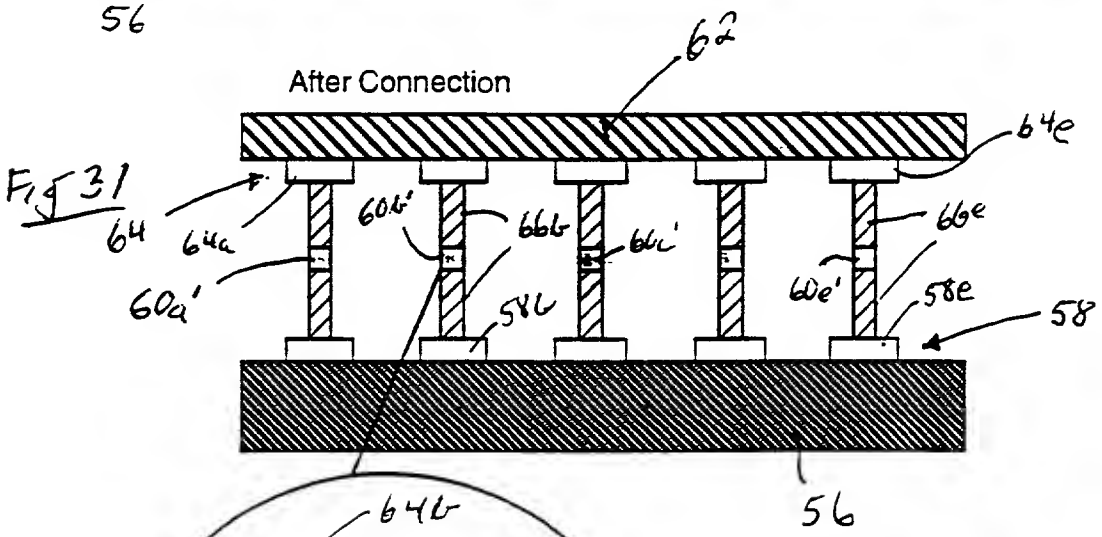
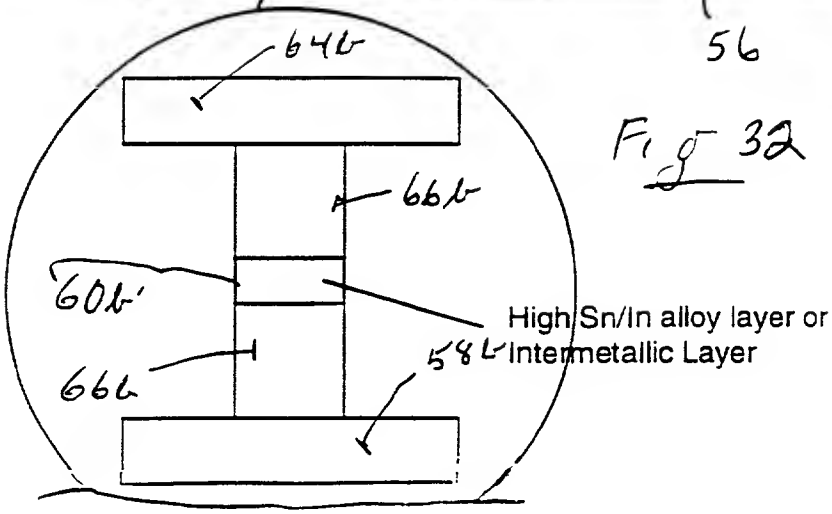


Fig 32



Structure 4: Cup-TLB

Fig 33

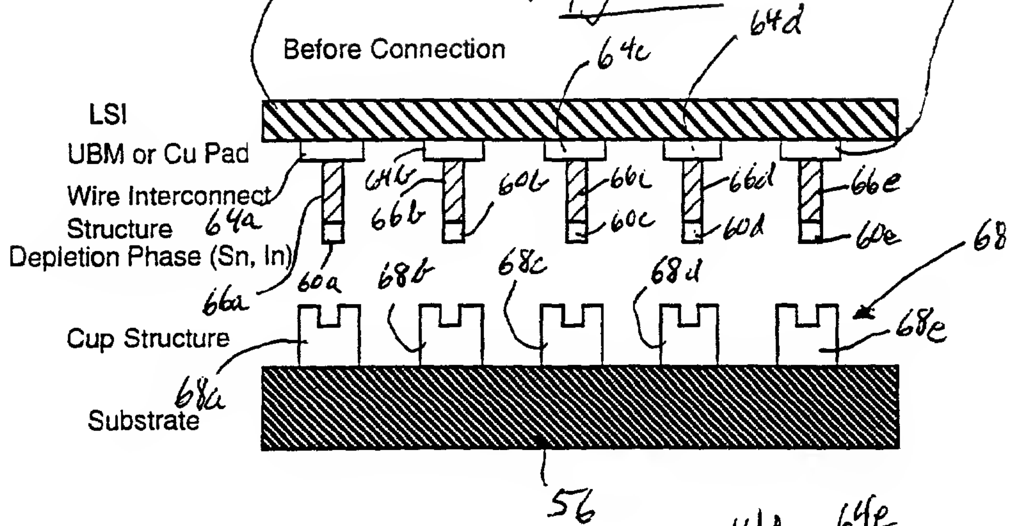


Fig 34

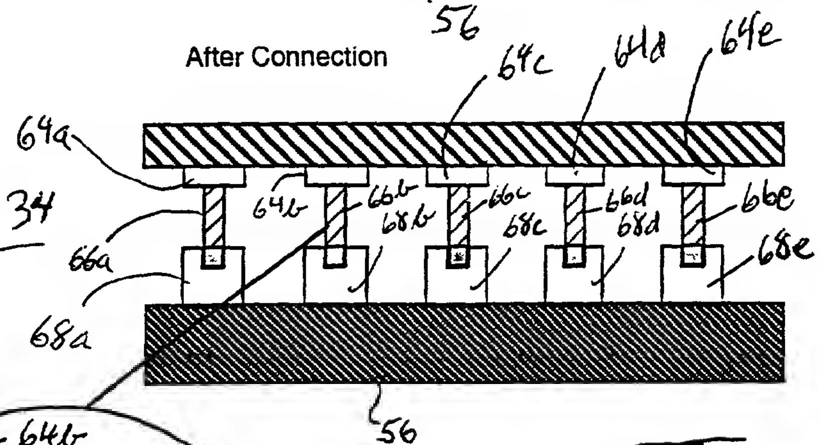


Fig 36

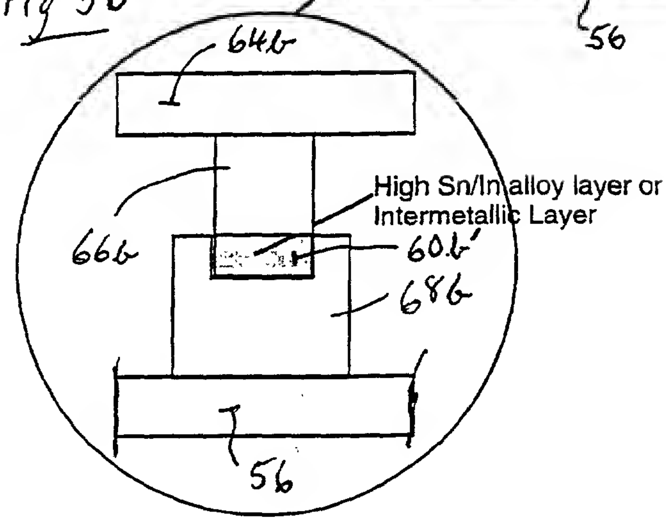
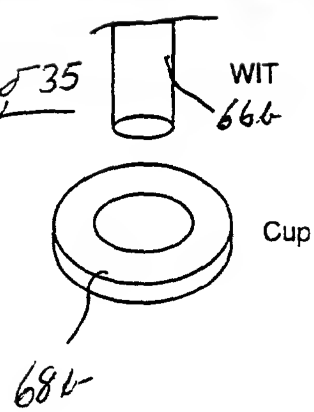


Fig 35



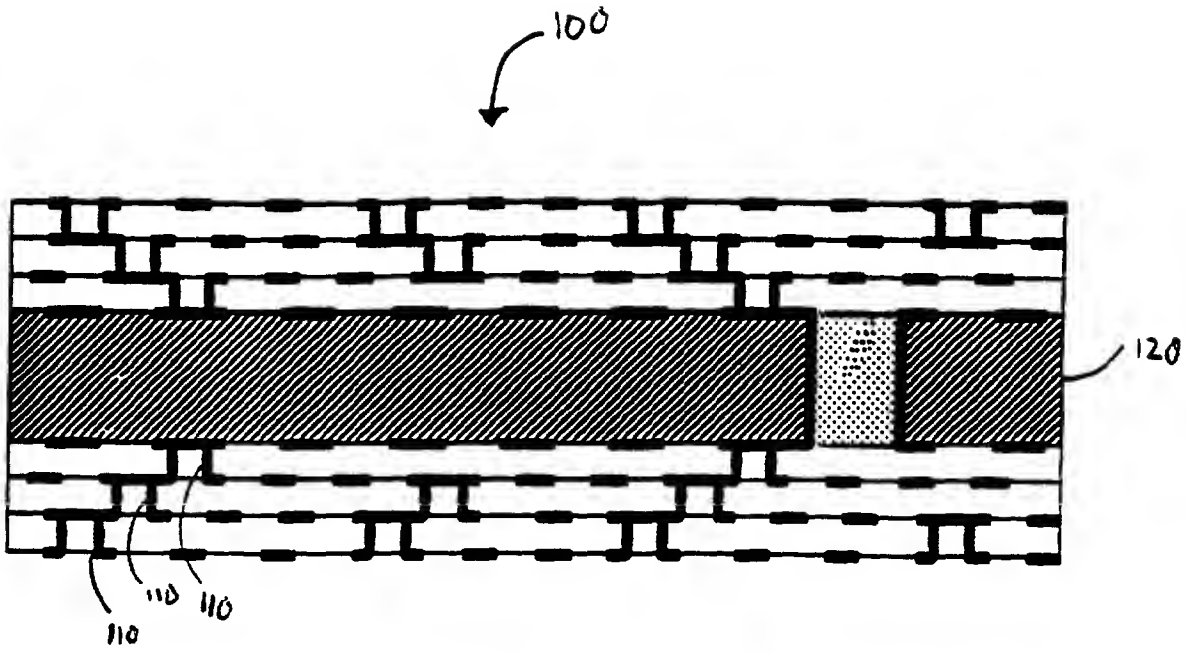


FIG.3J

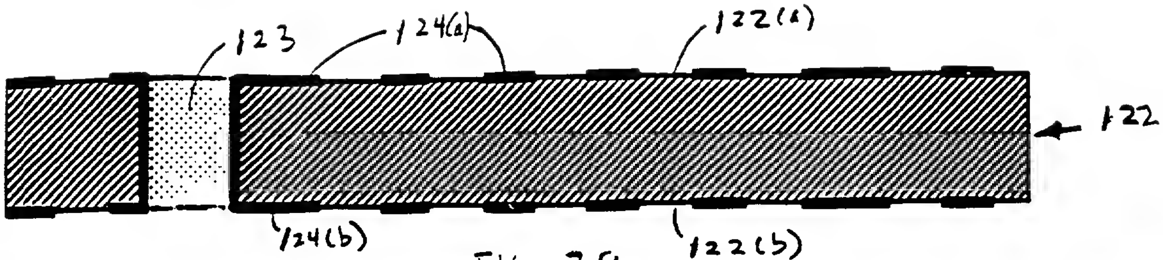


FIG. 38

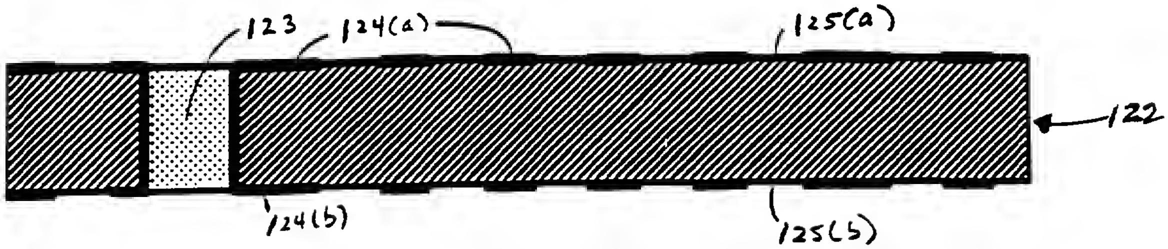


FIG. 39

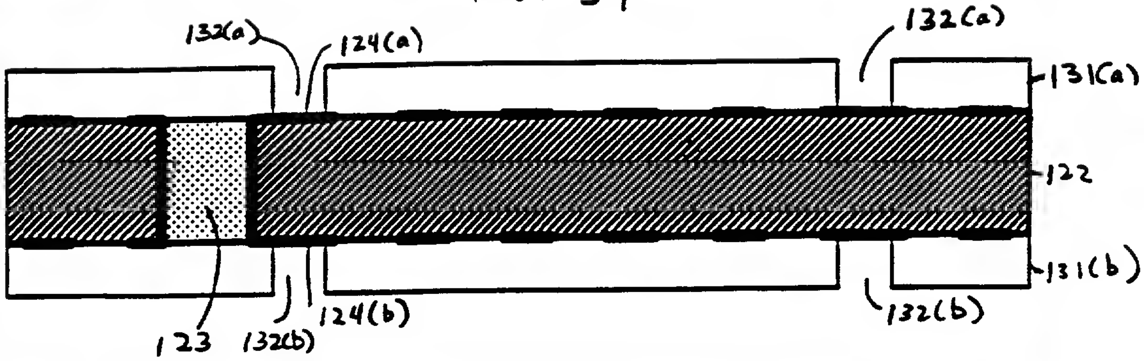


FIG. 40

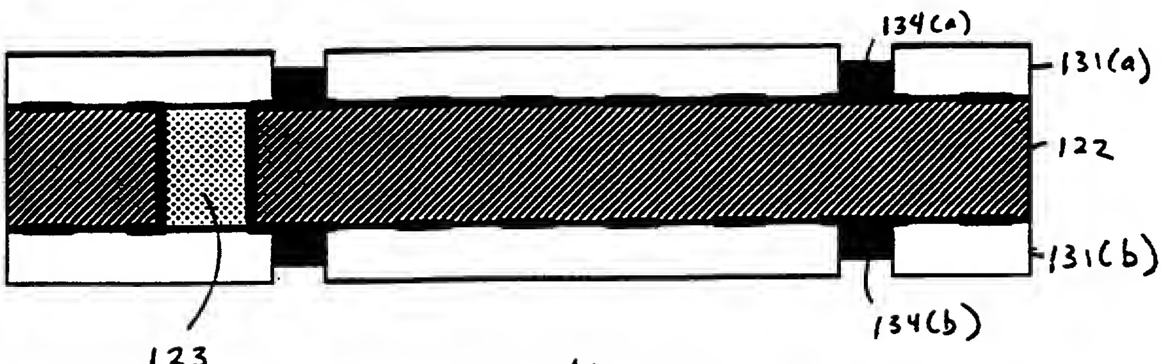


FIG. 41

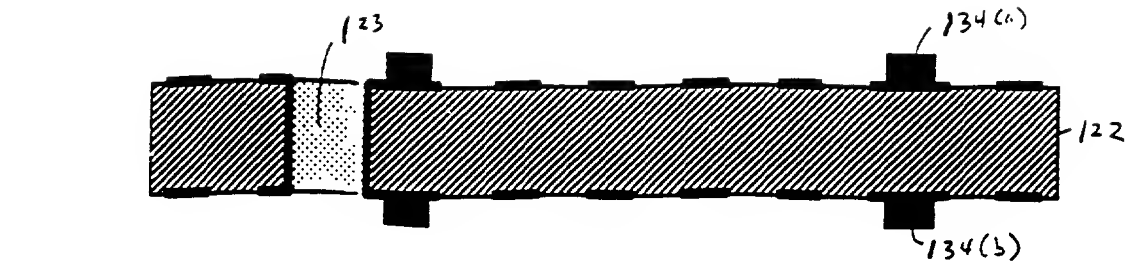


FIG. 42

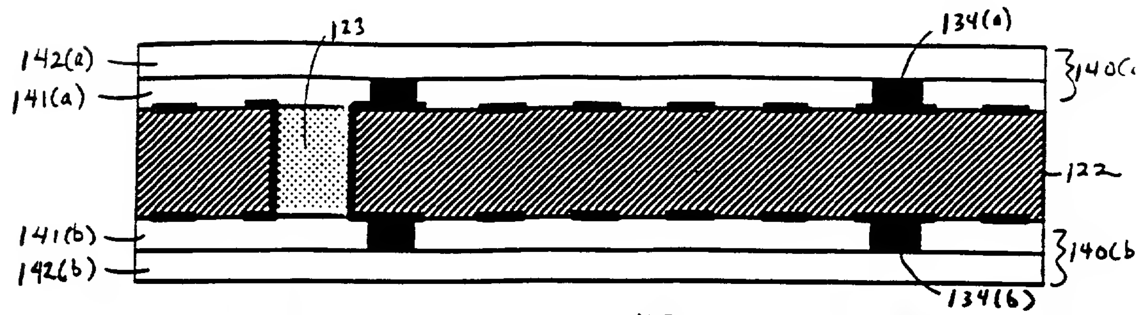


FIG. 43

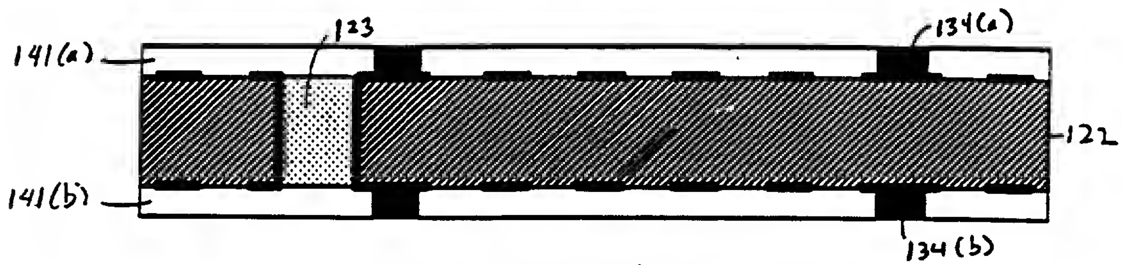


FIG. 44

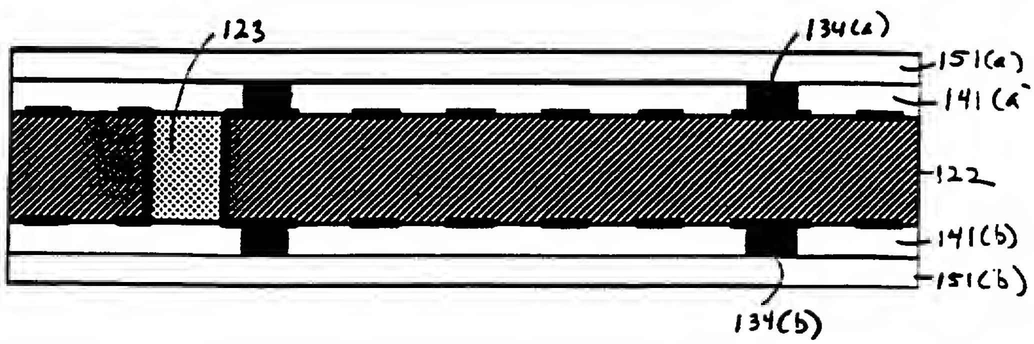


FIG. 45

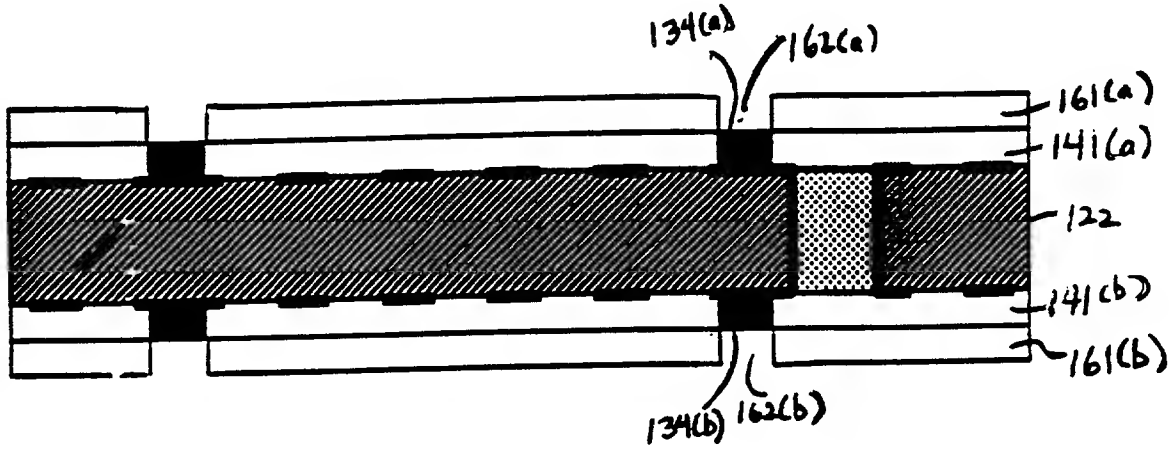


FIG. 46

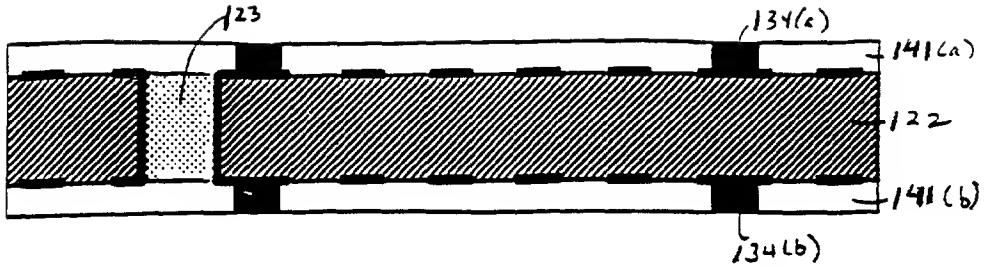


FIG. 47

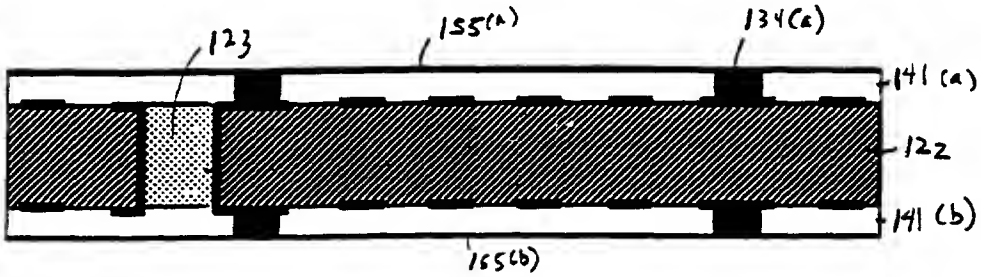


FIG. 48

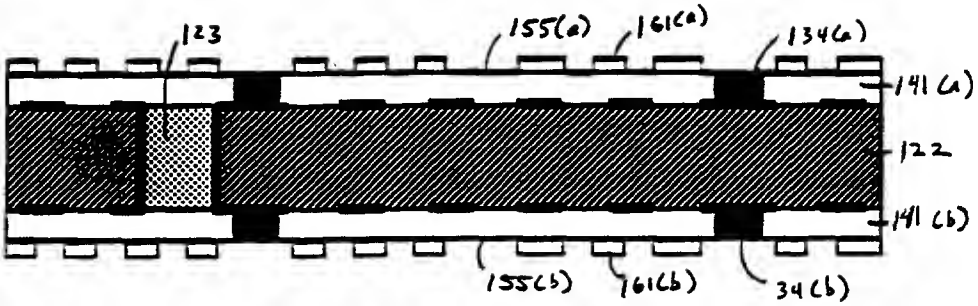


FIG. 49

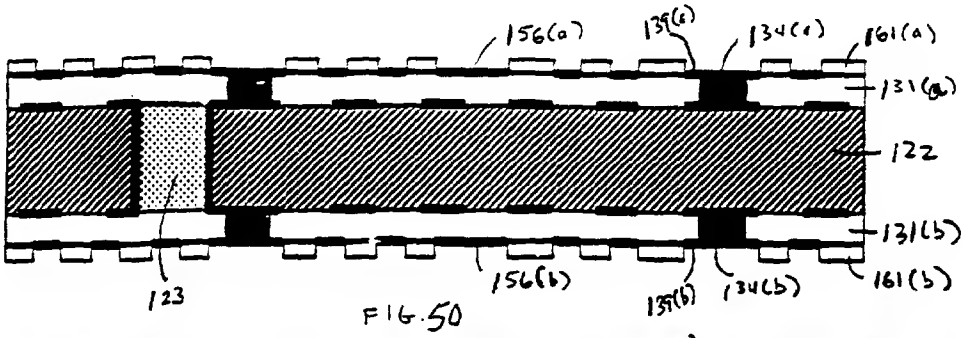


FIG. 50

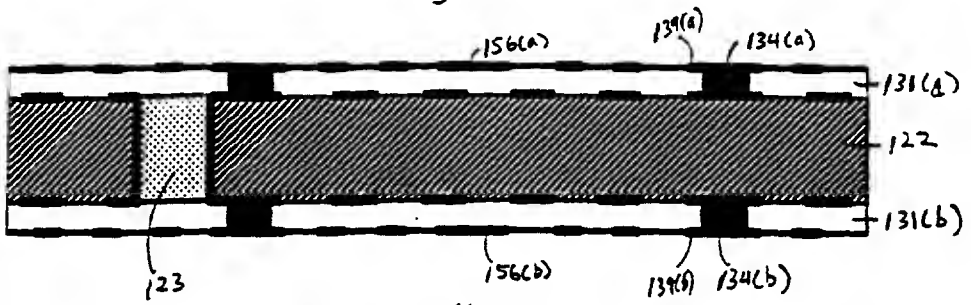


FIG 51

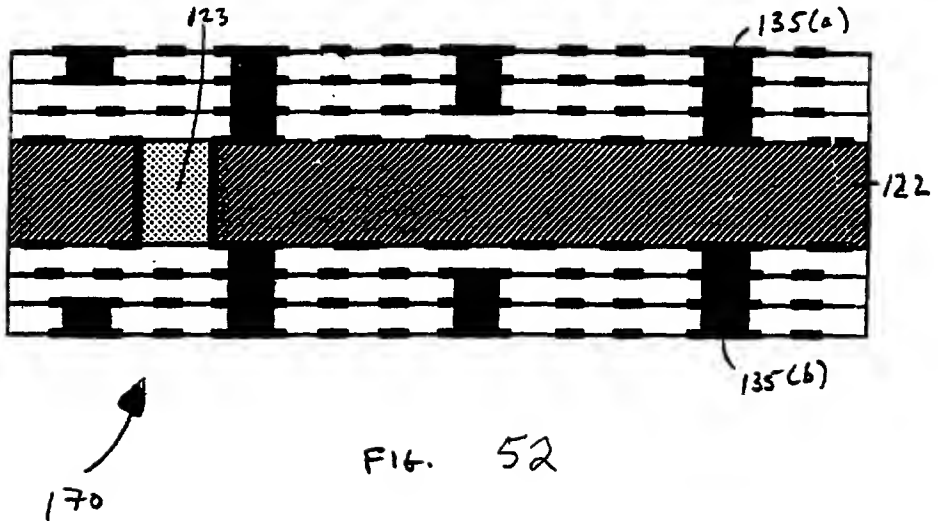


FIG. 52

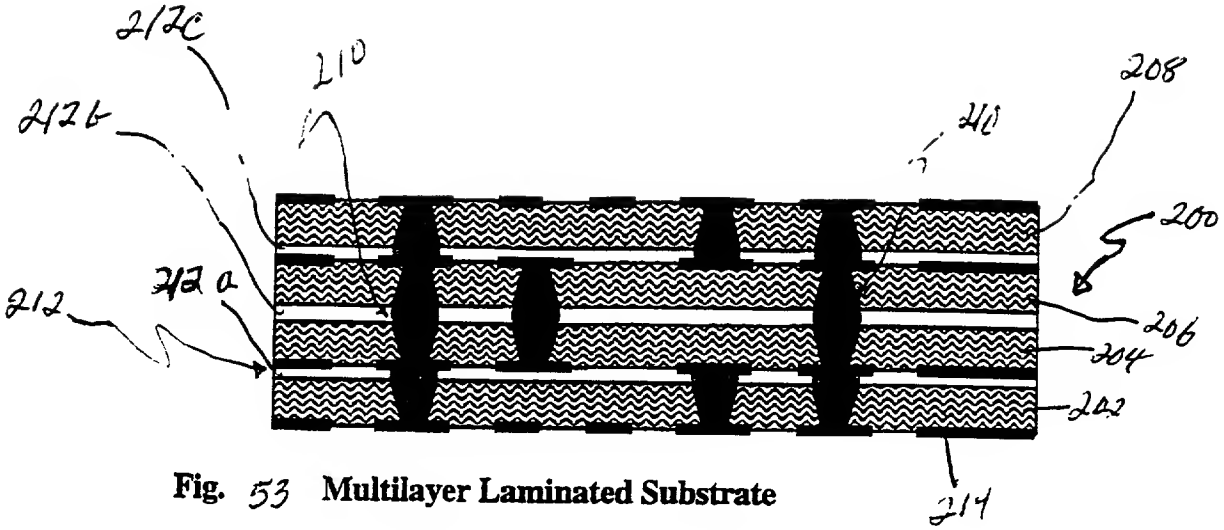


Fig. 53 Multilayer Laminated Substrate

Fabrication Flow – Subtractive

Fig. 54 Start from single side laminate

Fig. 55 Laser blind via

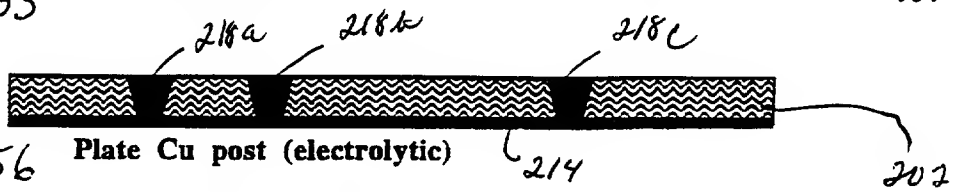


Fig. 56 Plate Cu post (electrolytic)

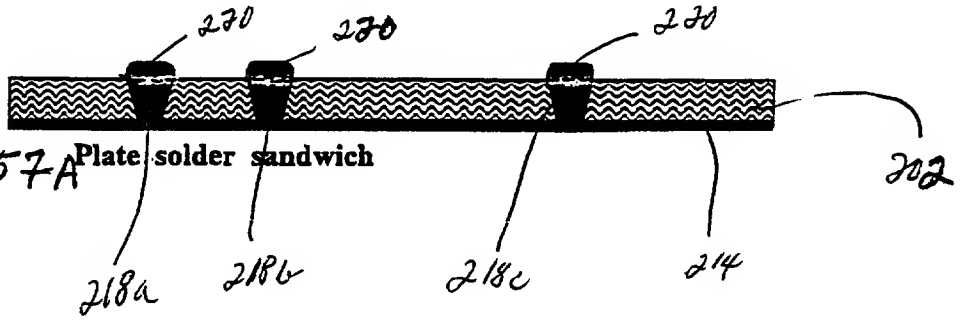
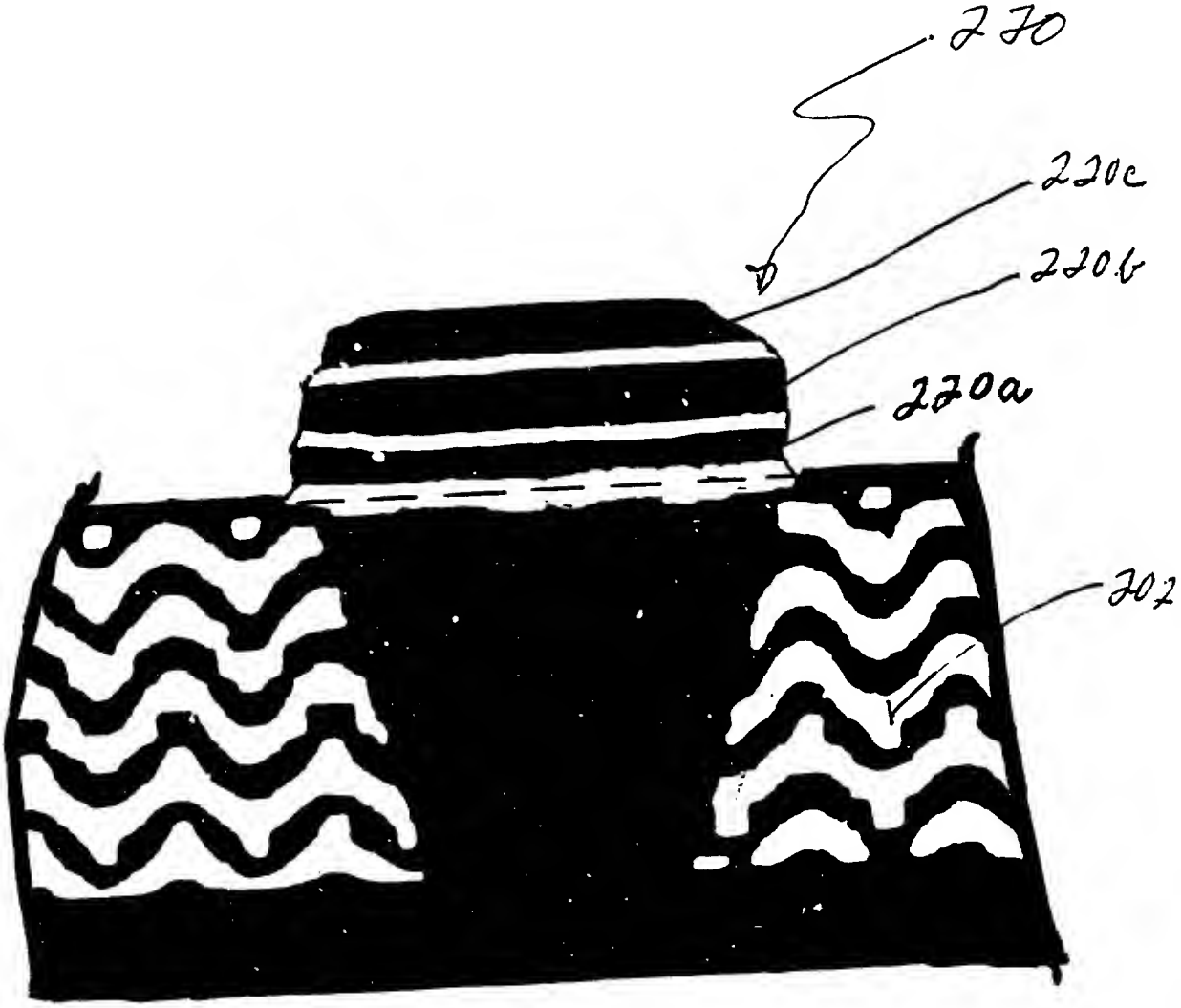
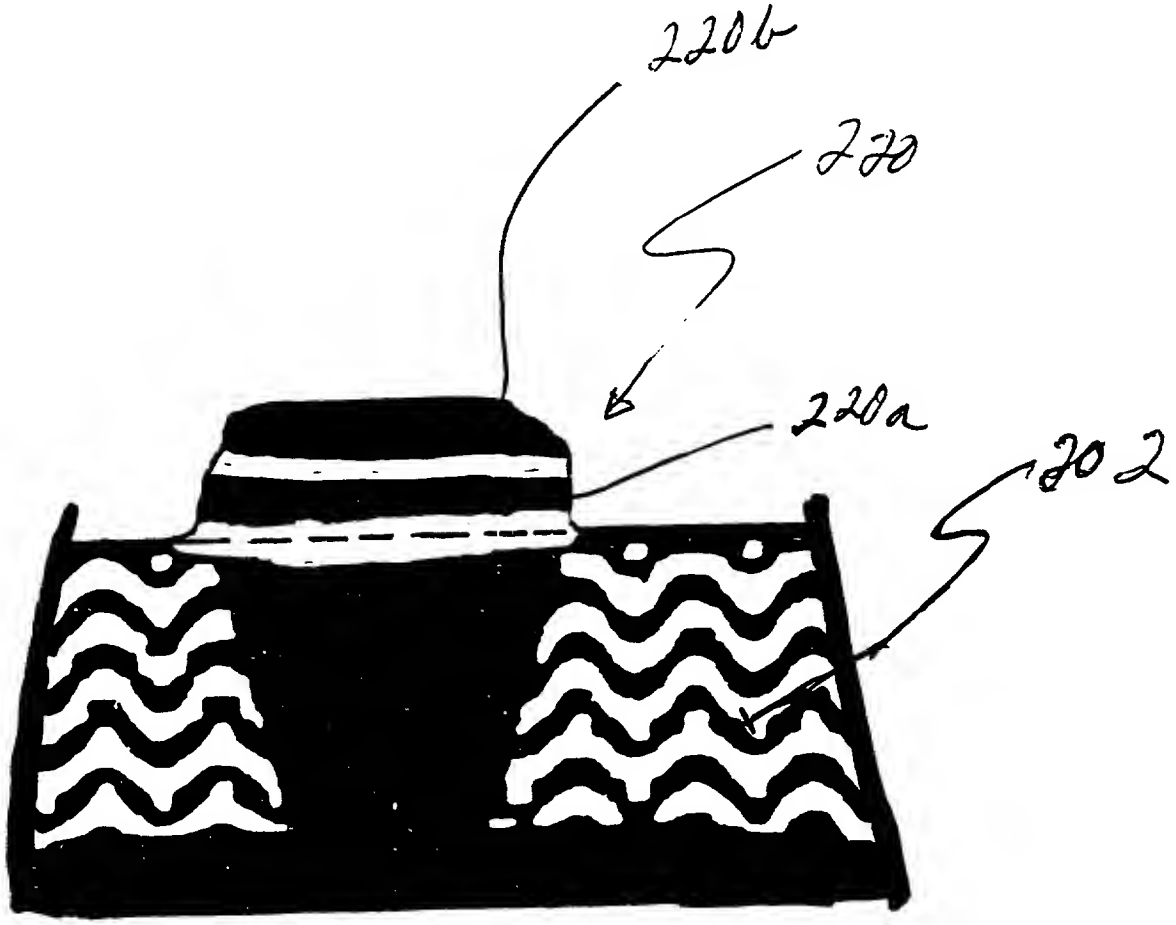


Fig. 57A Plate solder sandwich



5 7 B



57C

Option A:

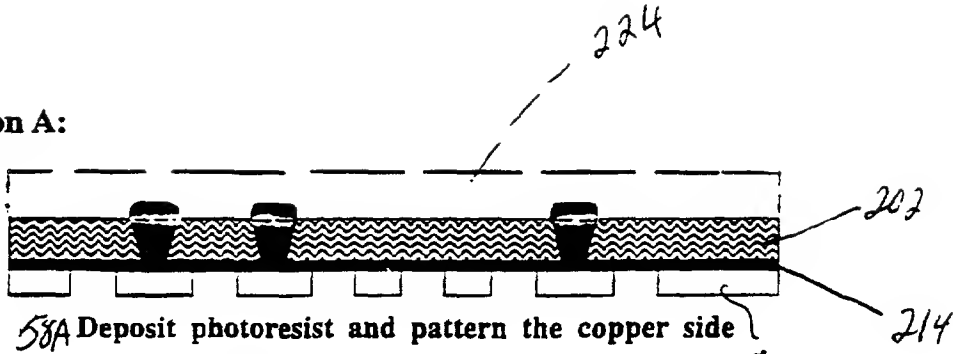


Fig. 58A Deposit photoresist and pattern the copper side

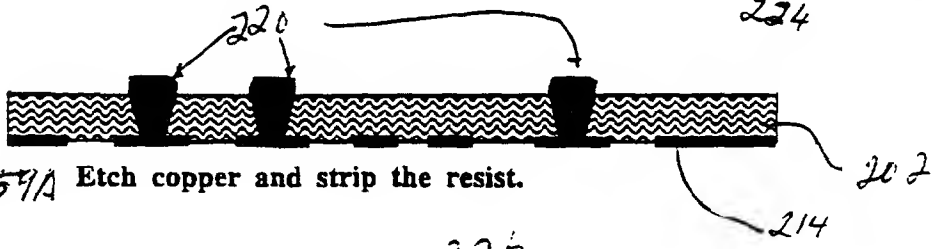


Fig. 59A Etch copper and strip the resist.

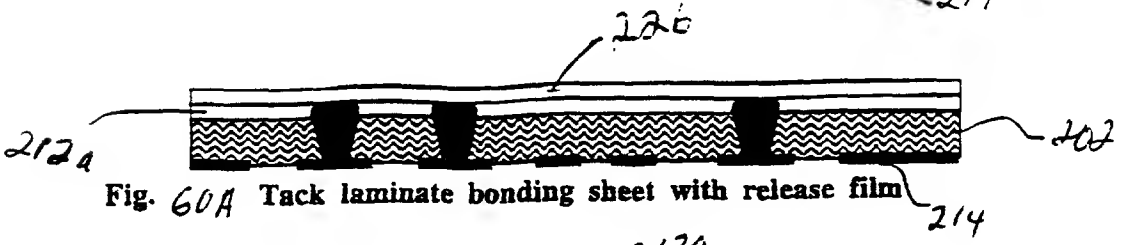


Fig. 60A Tack laminate bonding sheet with release film

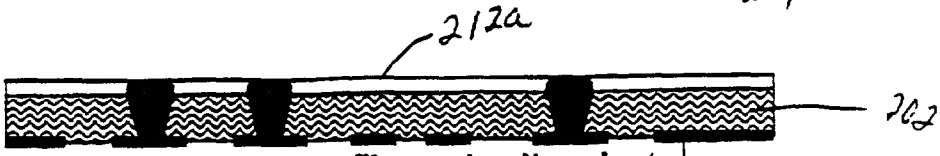


Fig. 61A Remove the release film on bonding sheet

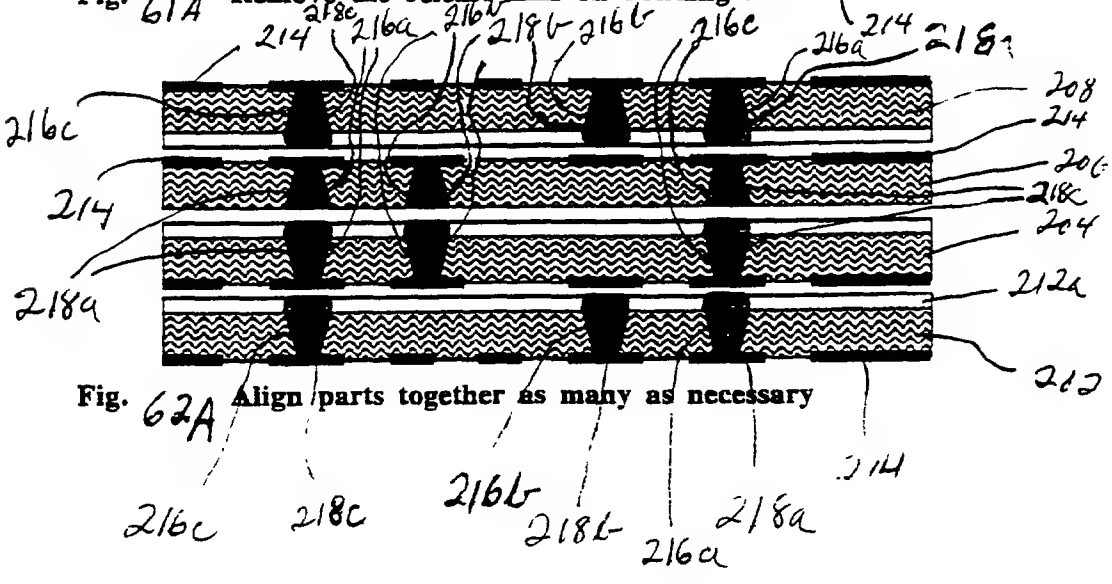


Fig. 62A Align parts together as many as necessary

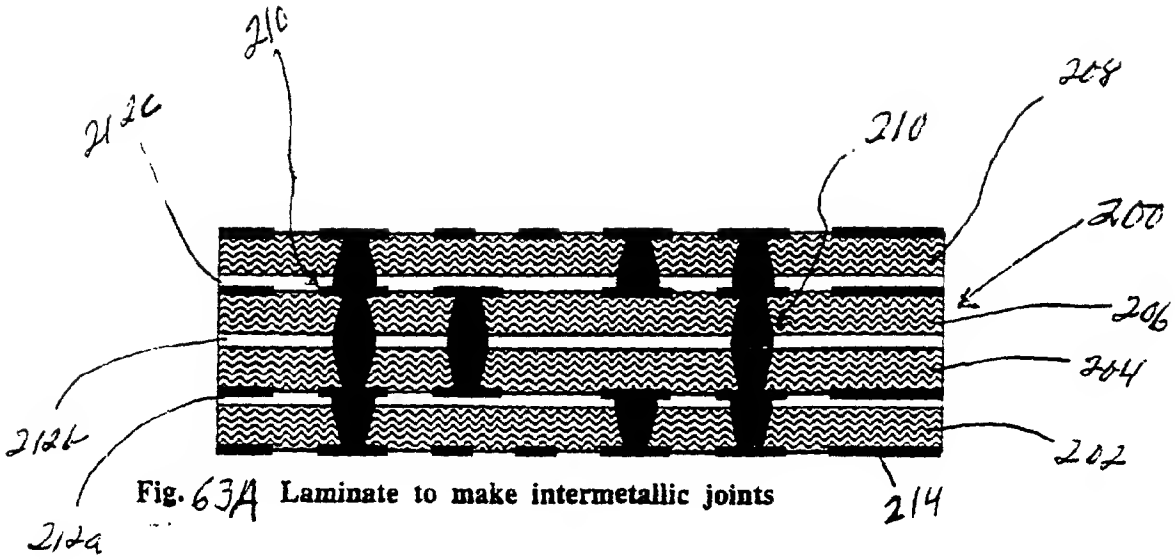


Fig. 63A Laminate to make intermetallic joints

Option B:

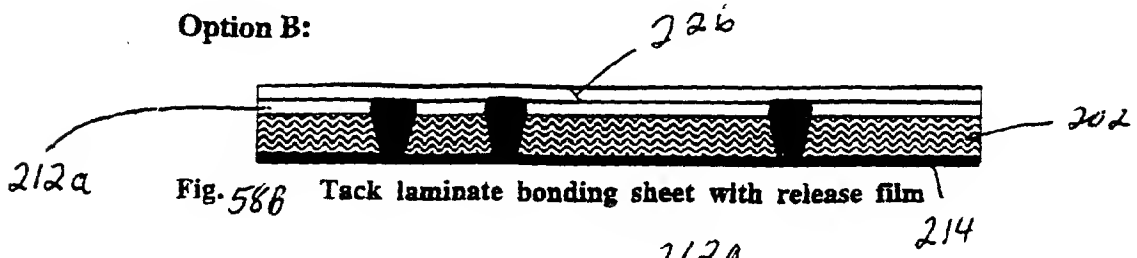


Fig. 58B Tack laminate bonding sheet with release film

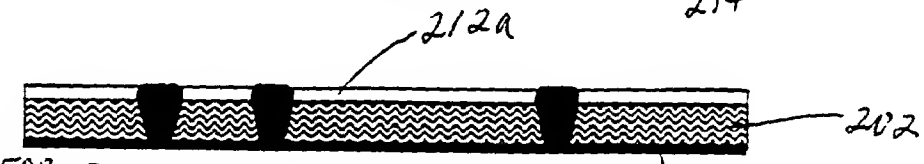


Fig. 59B Remove the release film on bonding sheet

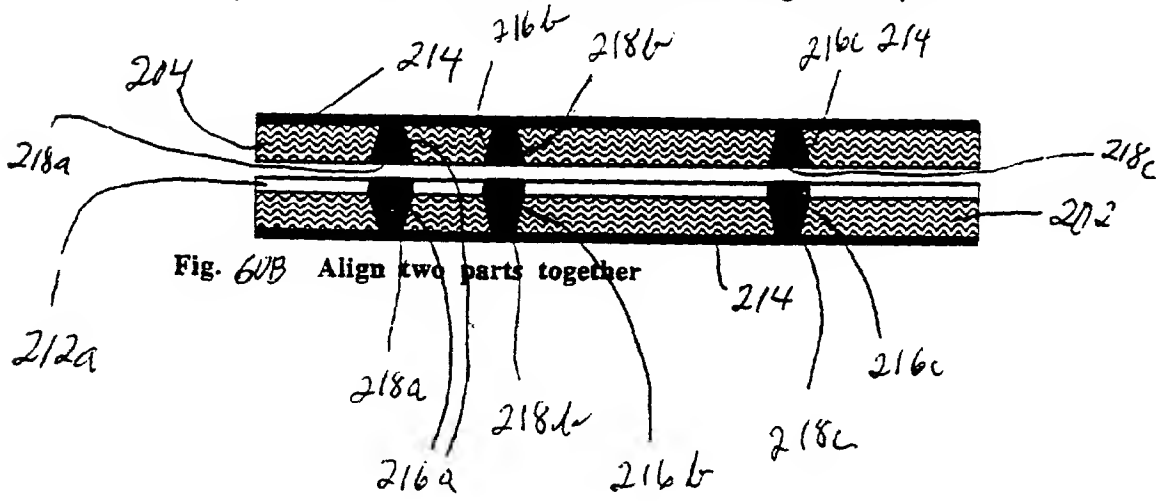


Fig. 60B Align two parts together

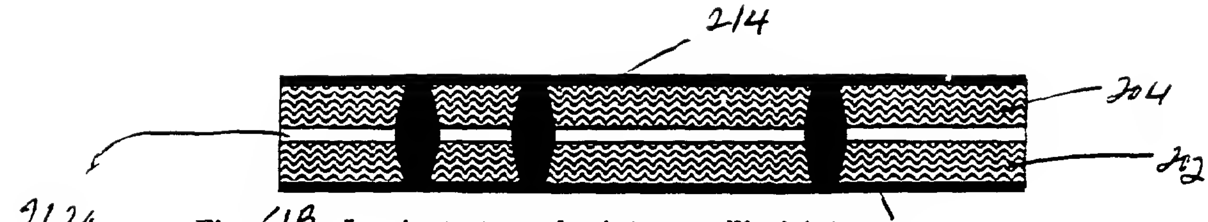


Fig. 61B Laminate to make intermetallic joints

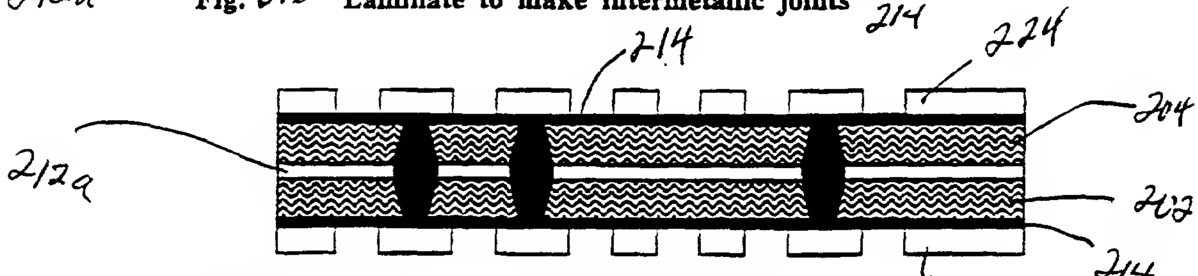


Fig. 62B Pattern by photoresists lithograph

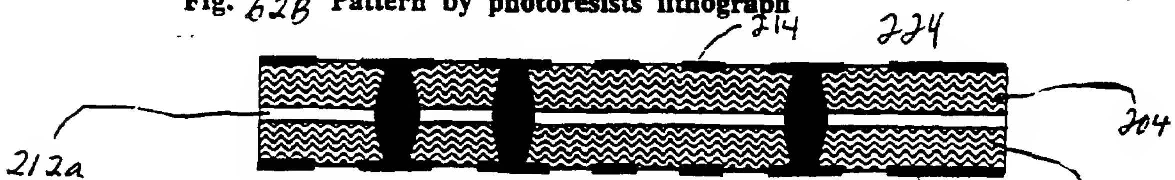


Fig. 63B Etch Cu and strip the resists

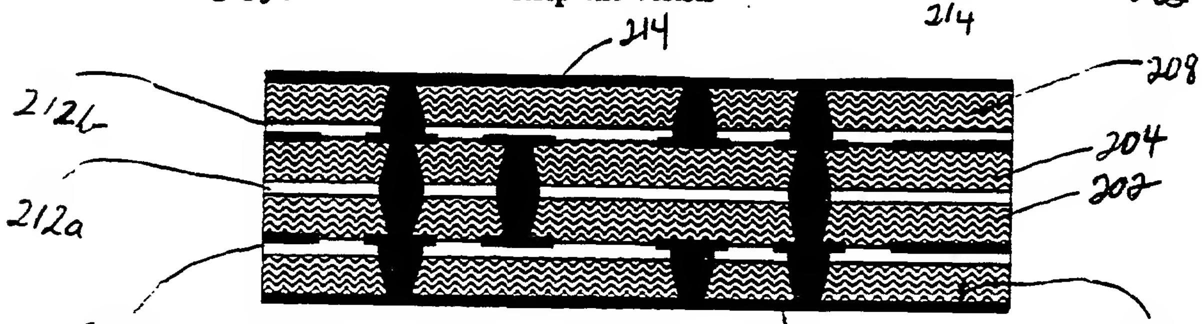


Fig. 64B Laminate 7b for more layers

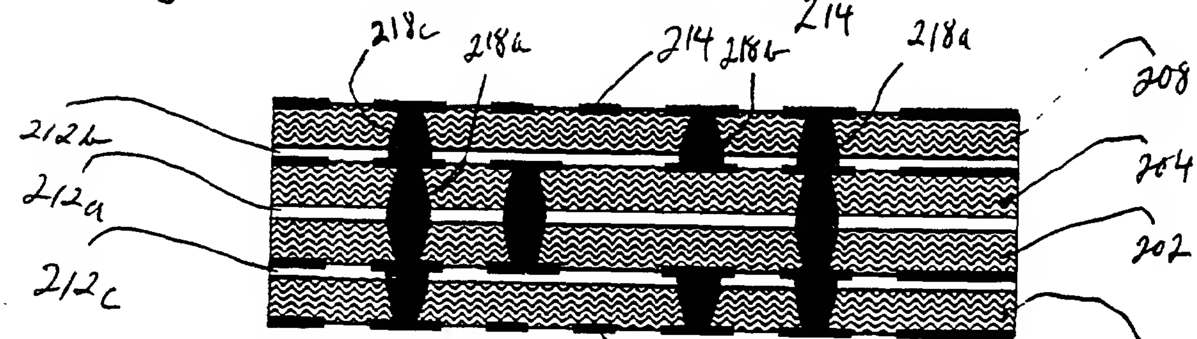
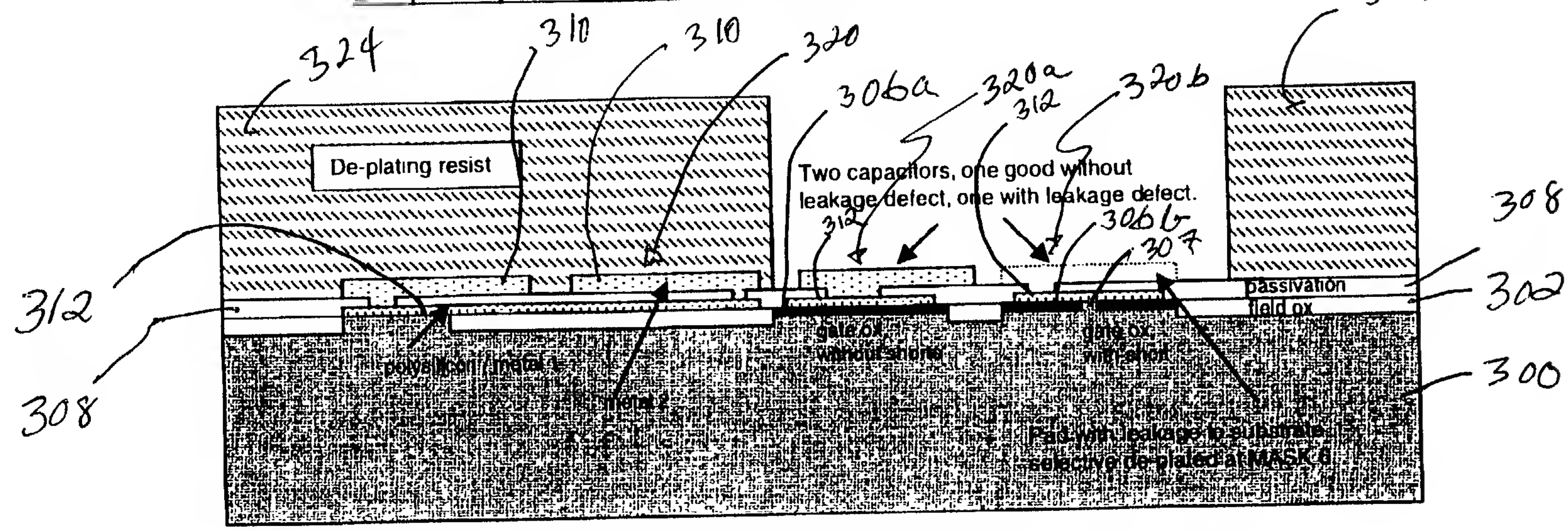


Fig. 65B Pattern Cu as 10b-11b 214

De-plate pads to capacitors with shorts



Process: Use a de-plating process to remove M2 pads connected to defective capacitors with shorts (or high leakage) to the substrate. M2 is copper. Mask design opens resists over the entire M2 capacitor pads, or only the trace leading to the pad. Breaking the capacitor into many small capacitors, allows the isolation (de-plating) of defects without large reductions in capacitiance

Fig 66

- process completed thru Metal 2.
- spin resist
- de-plate (MASK 6) — Mask design opens resists over all M2 capacitor pads
- de-plate defective capacitors — Place wafer in plating fixture and put in plating solution. The plating bias is the reverse that used to plate copper, negative voltage to back of wafer and positive voltage to solution. Plating solution can be copper sulfate, sulfuric acid, and additives. Contact to the back of the wafer can be from therontside ; M2 pads to metal 1 to the silicon.
- wet etch — with resist on, follow deplate with short Cu etch to remove residue. The adhesion layer etch, to remove any exposed adhesion layer.
- strip resist

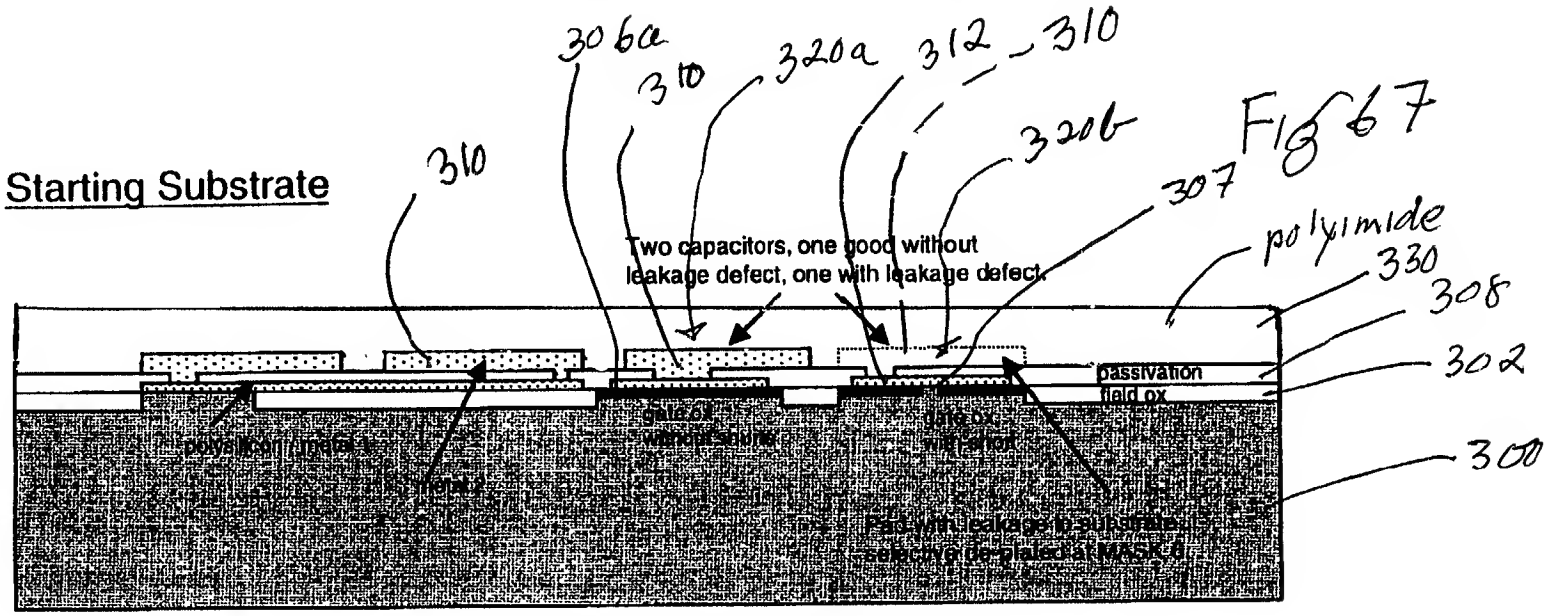


Fig 67

Semiconuctor process:
- nitride deposition
- field oxide (MASK 1)
- nitride etch, field oxidation(1um), nitride stripe, gate oxidation(10nm)
- contact mask (MASK 2)
- oxide etch, polysilicon deposit, metal deposit
- metal 1 mask (MASK 3)
- aluminum etch, polysicon etch, passivation deposition
- pad mask (MASK 4)
- passivation etch, TiCu deposition
- metal 2 mask (MASK 5)
- M2 pattern
- de-plate (MASK 6)
- de-plate defective capacitors
- polyimide coat

Fig 67

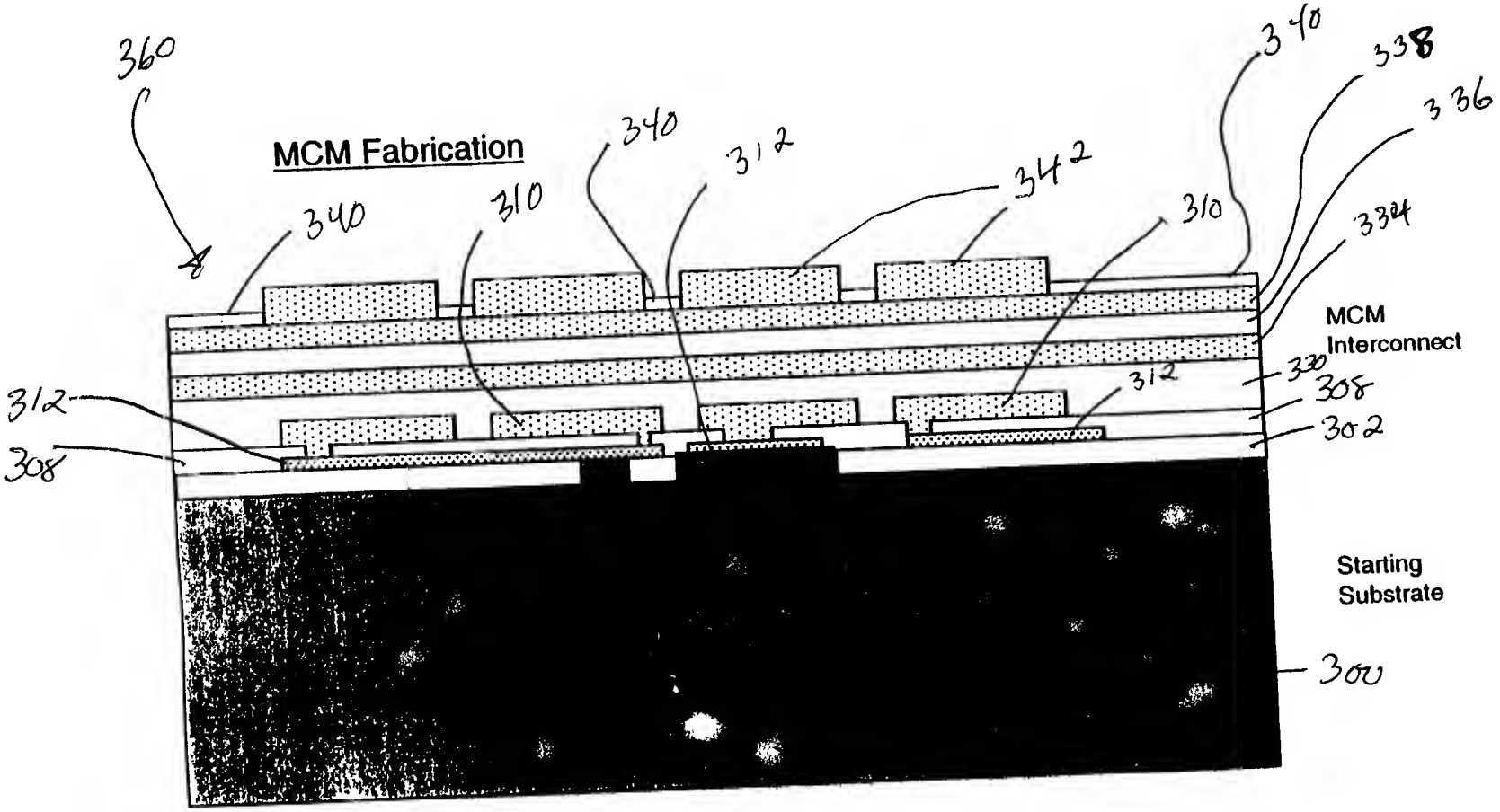
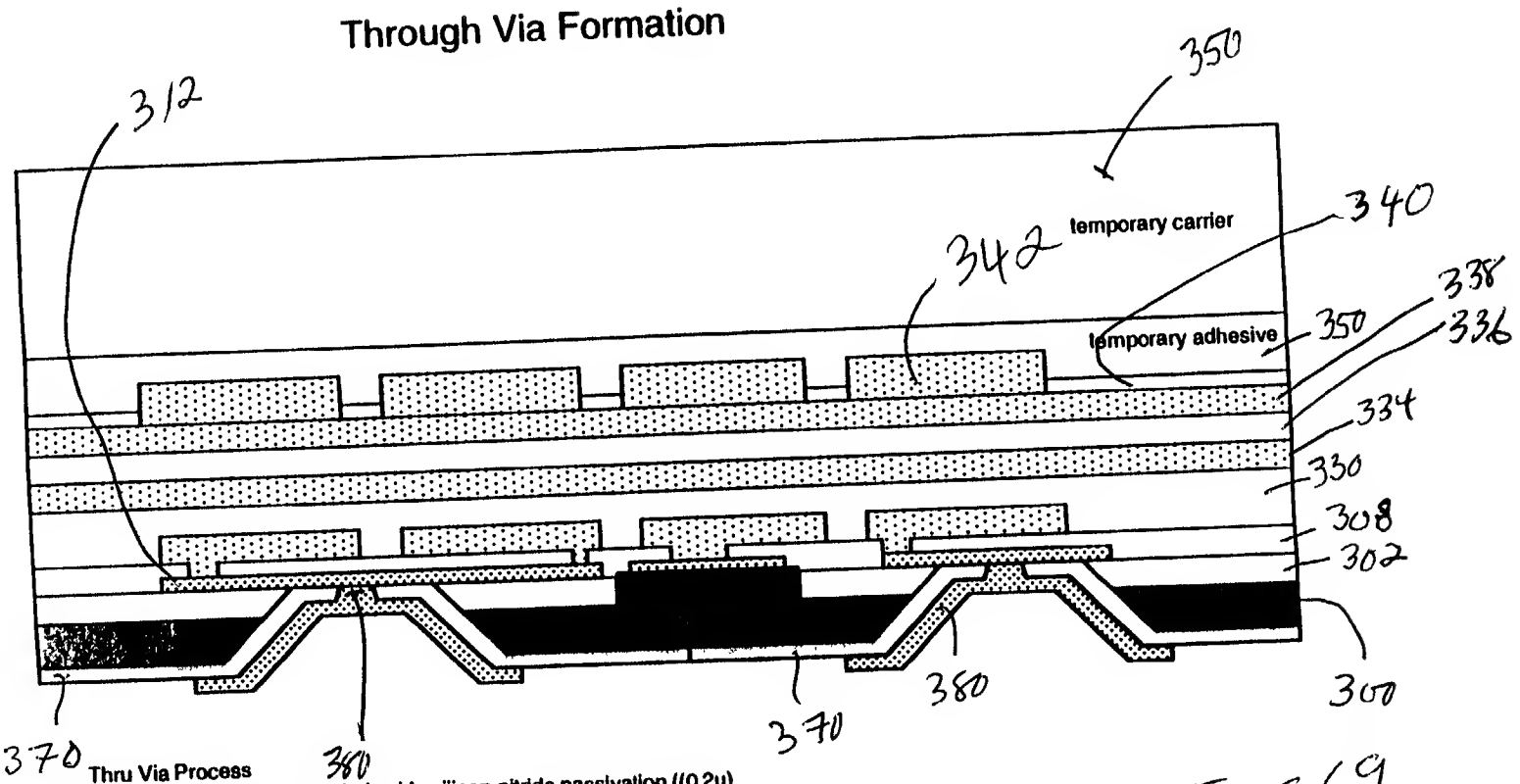


Fig 68



Thru Via Process
- backgrind wafer to 200u, bakcside silicon nitride passivation ((0.2u)
- mount temporary carrier
- thru via (MASK 7)
- plasma etch nitride, KOH etch thru wafer (stop on field oxide), plasma etch oxide, polysilicon (stop on M1)
- vapor deposit parylene (20u), laser via in parylene, plasma clean via CrCu seed deposition
- via pad (MASK 8) using laminated resist
- Cu plate(10u), seed etch, eless Ni/Au plate

Fig 69

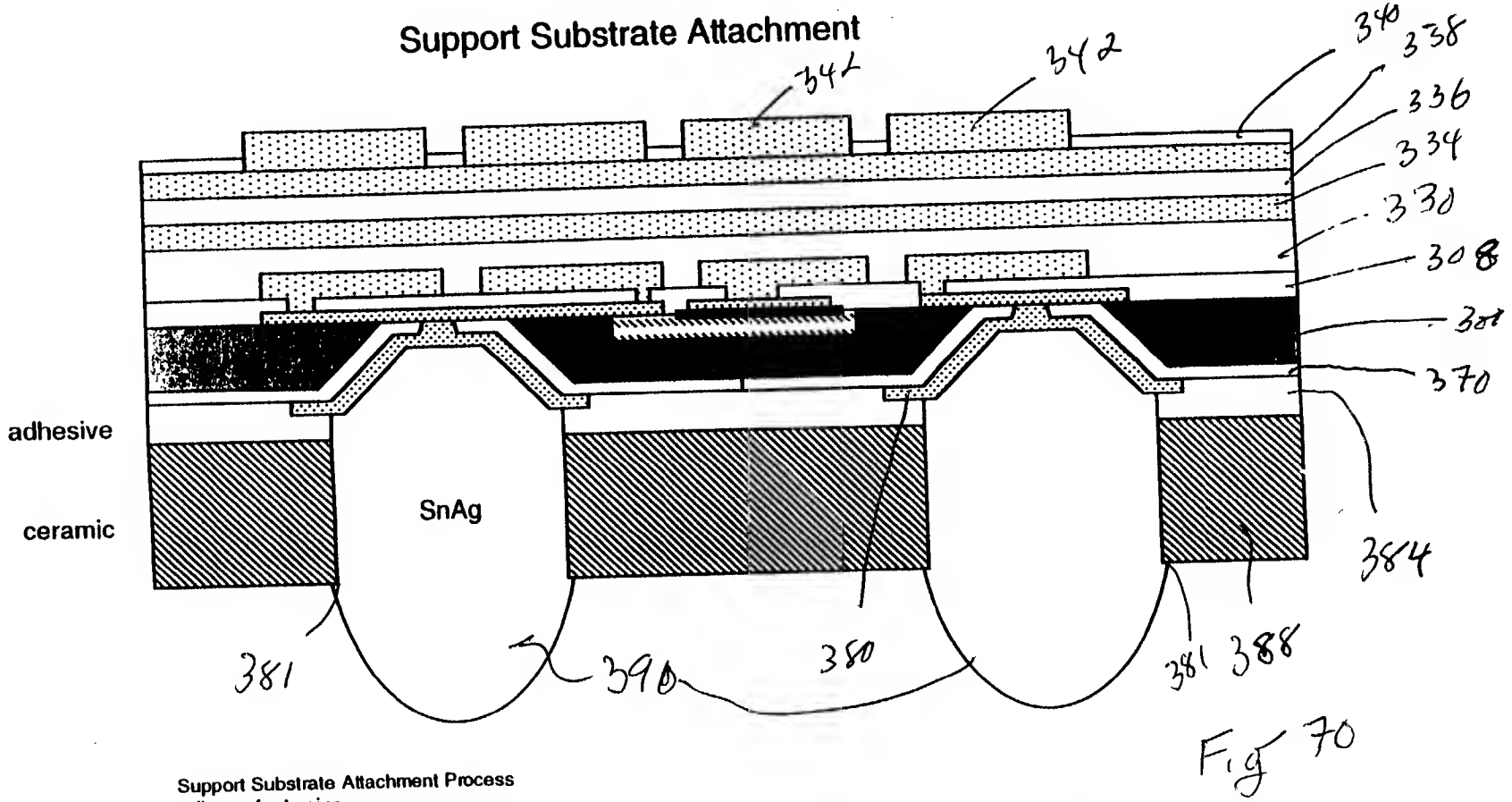


Fig 70

Support Substrate Attachment Process
- dice wafer to size
- tack adhesive to ceramic substrate with thru vias, use ceramic thru vias as laser mask to remove adhesive
- laminate ceramic to wafer
- screen SnAg paste into via holes, place SnAg solder balls to increase volume
- reflow solder

Alternate application: Active silicon substrate
with CPU die mounted over CMOS SRAM

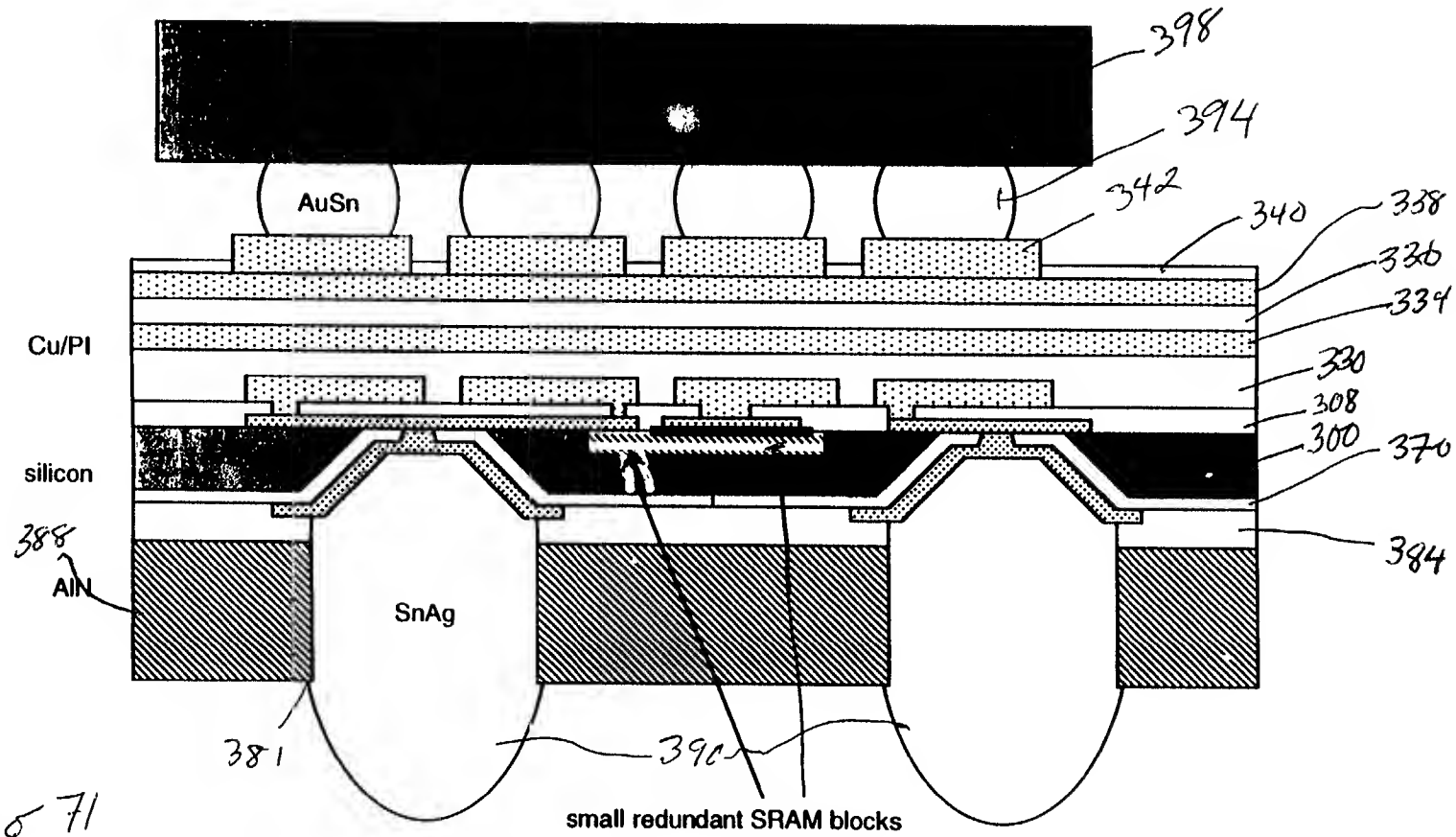
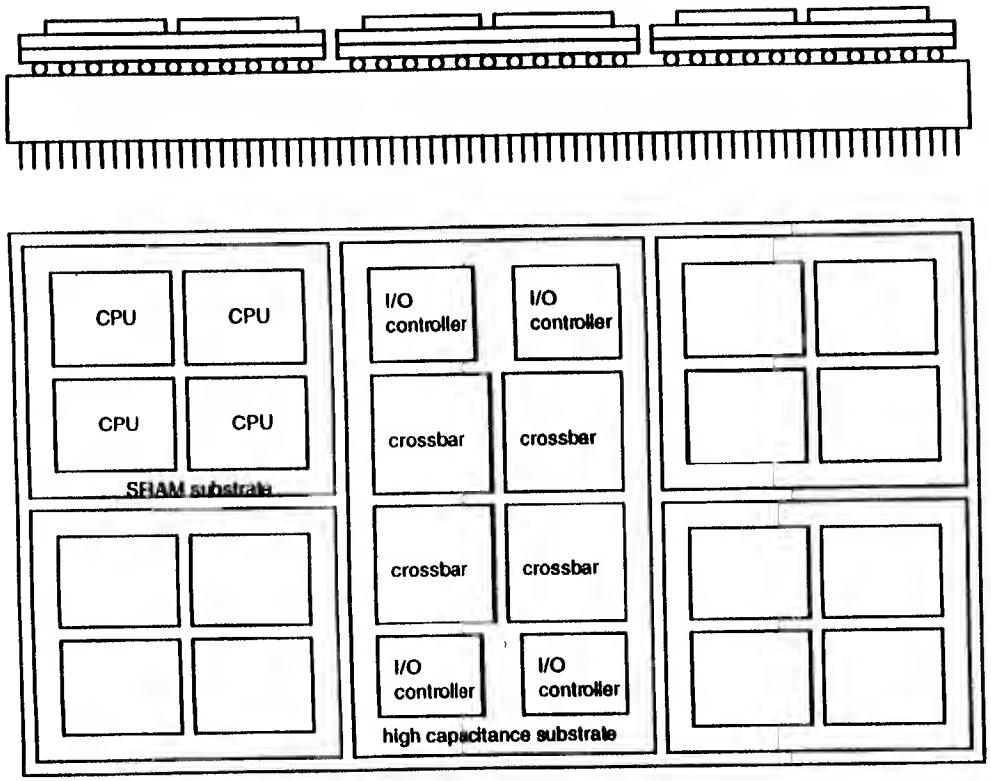


Fig 71

Alternate application with 3D SuperChip for high performance MCM



3D SuperChip

Conventional MCM

Fig 72

30x40mm
12 per 6" substrate

60x120mm
2 per 6" substrate

Fig 73

Alternate application with 3D SuperChip for 8-way server

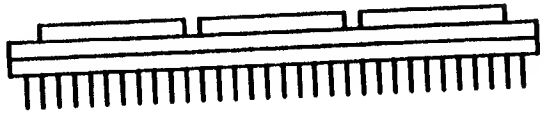
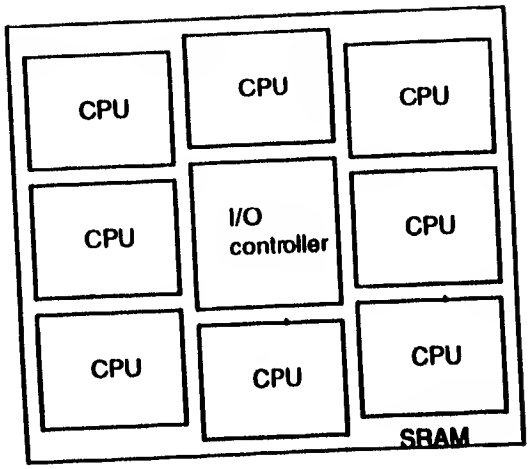


Fig 74



50 x 50 mm

Fig 75

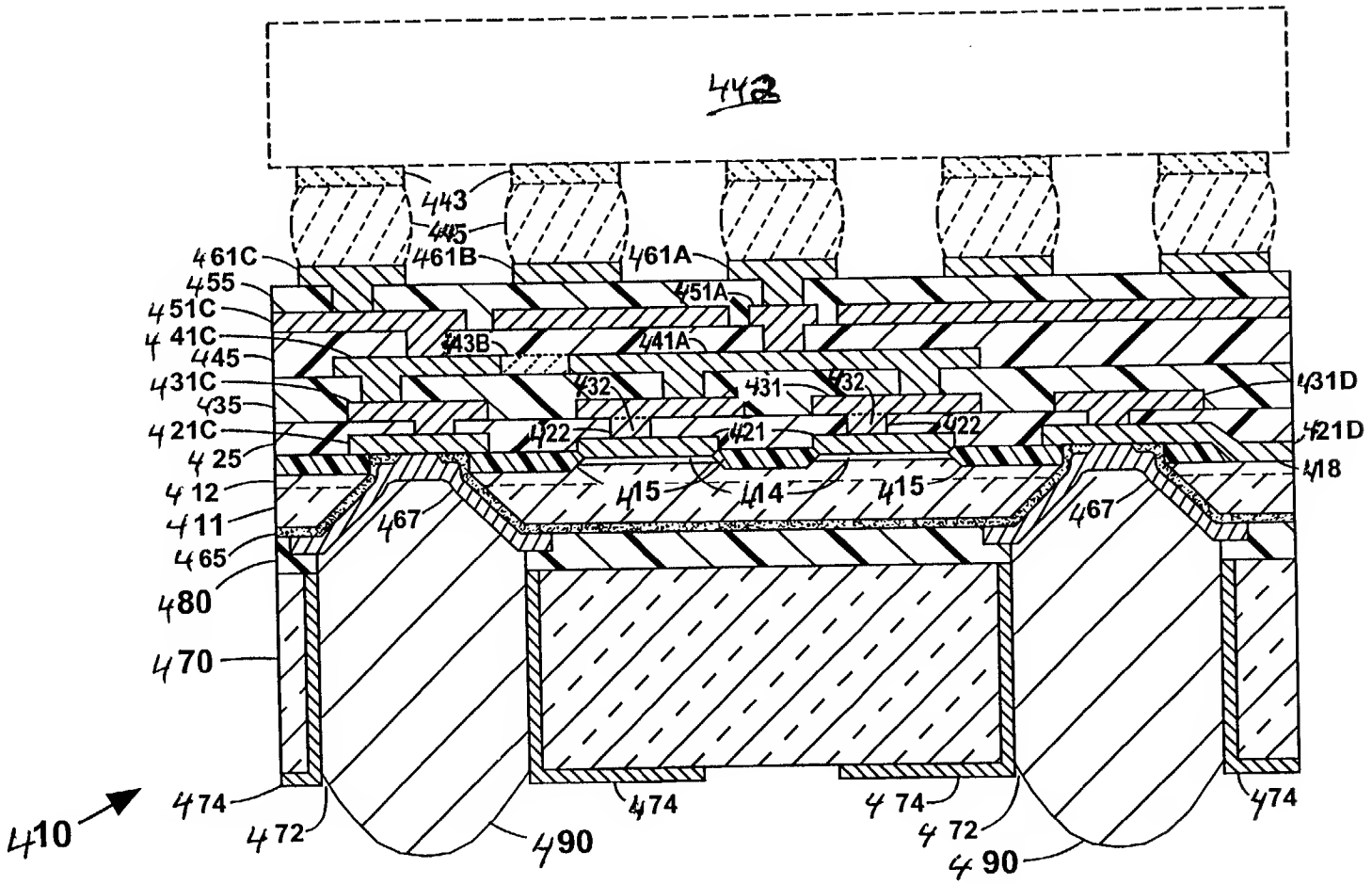


FIG. 76

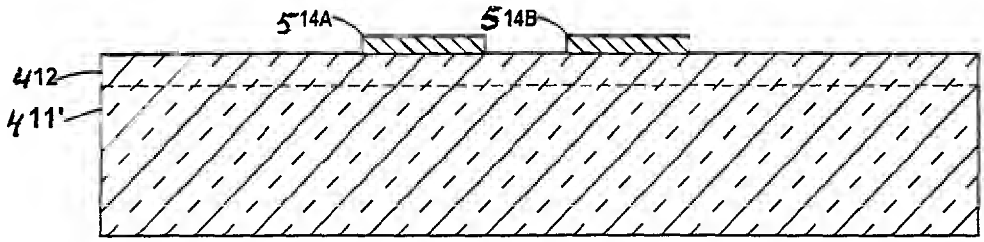


FIG. 77

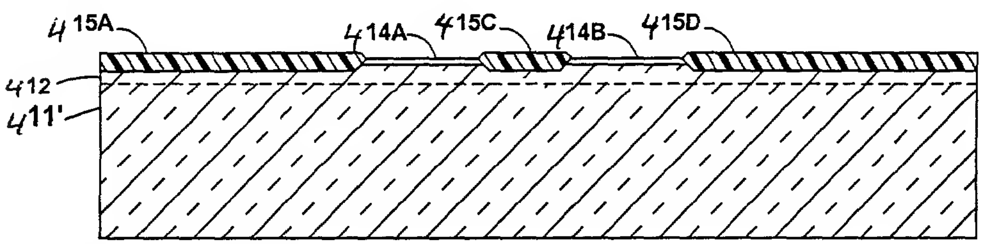


FIG. 78

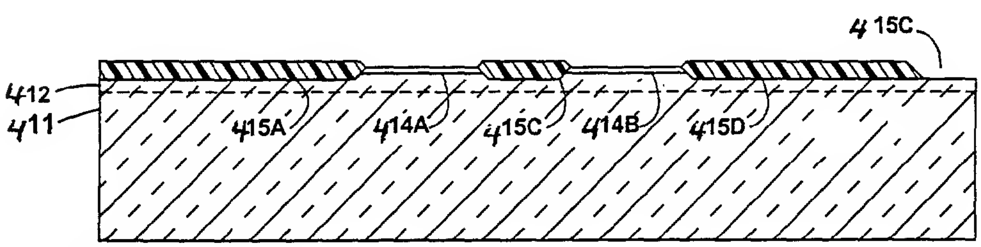


FIG. 79

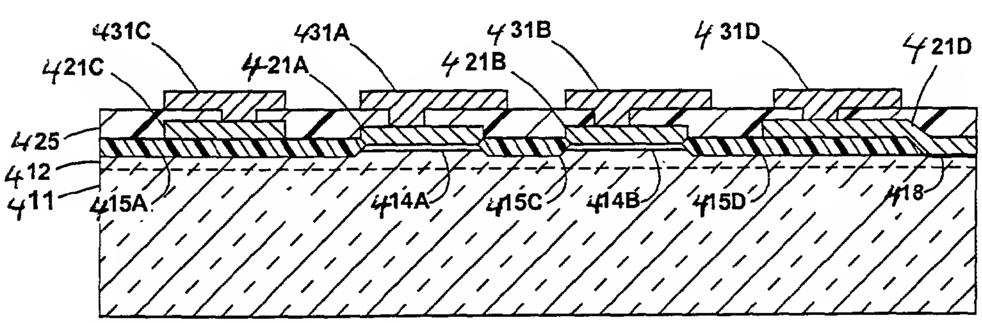


FIG. 80

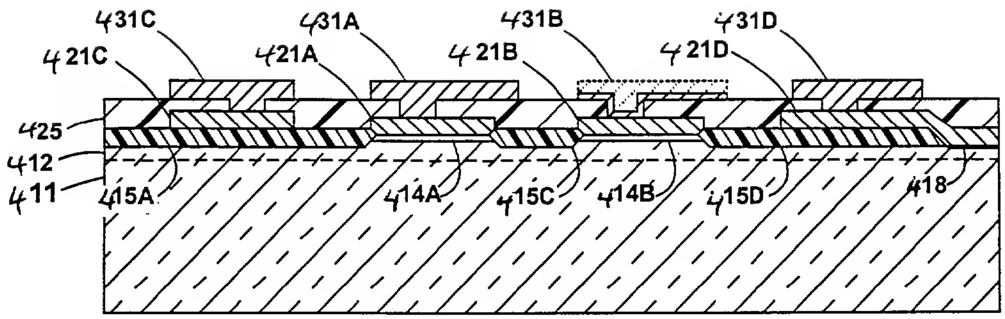


FIG. 81

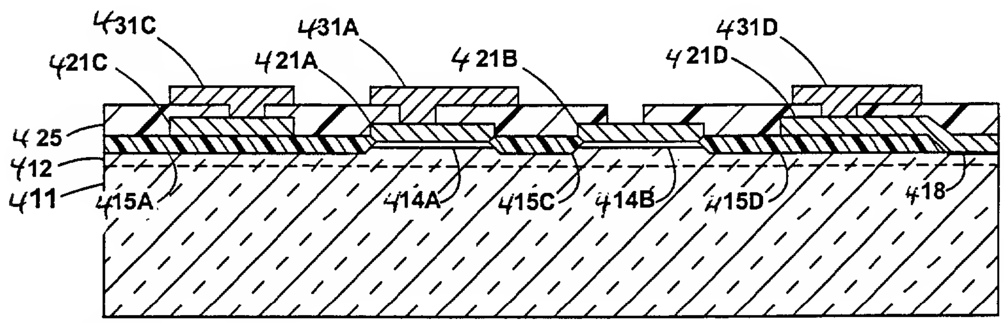


FIG. 82

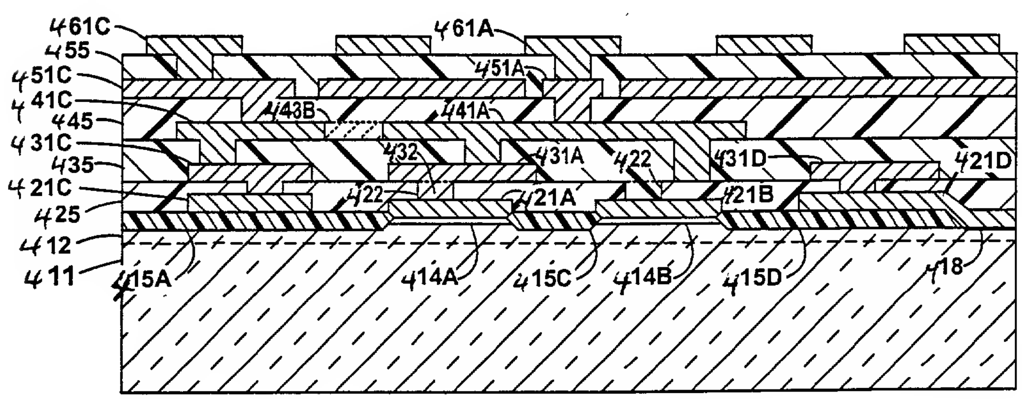
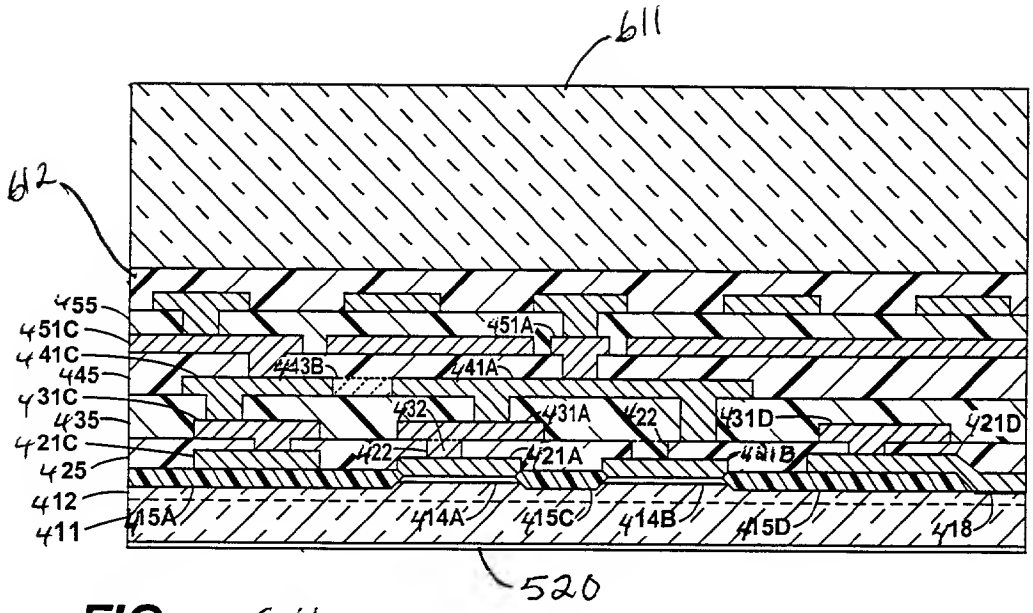


FIG. 83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421C
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415A
414A
415C
414B
415D
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520

FIG. 84

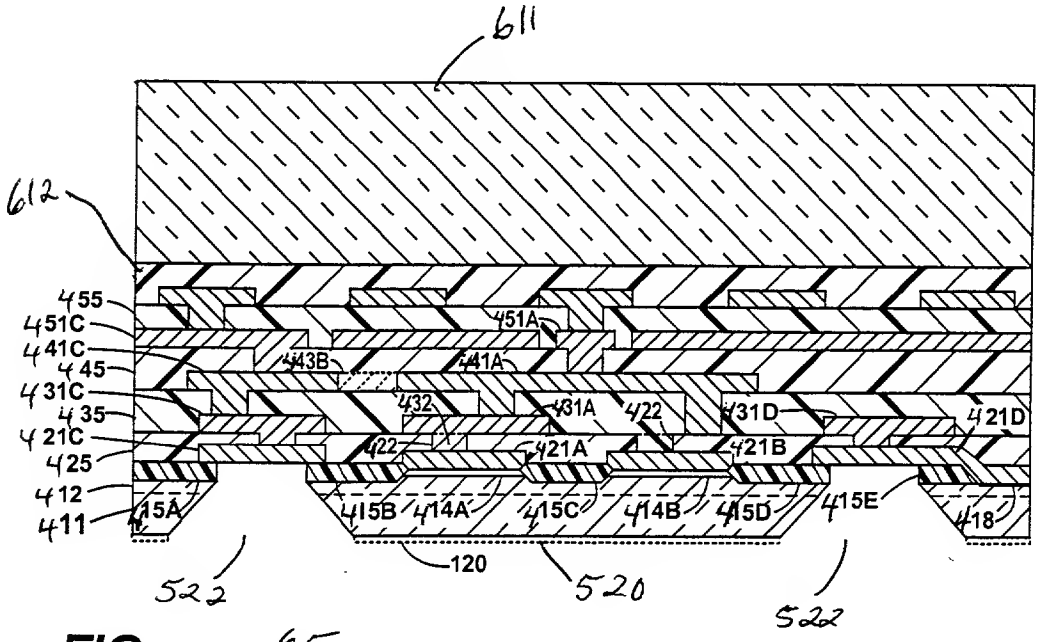
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FIG. 85

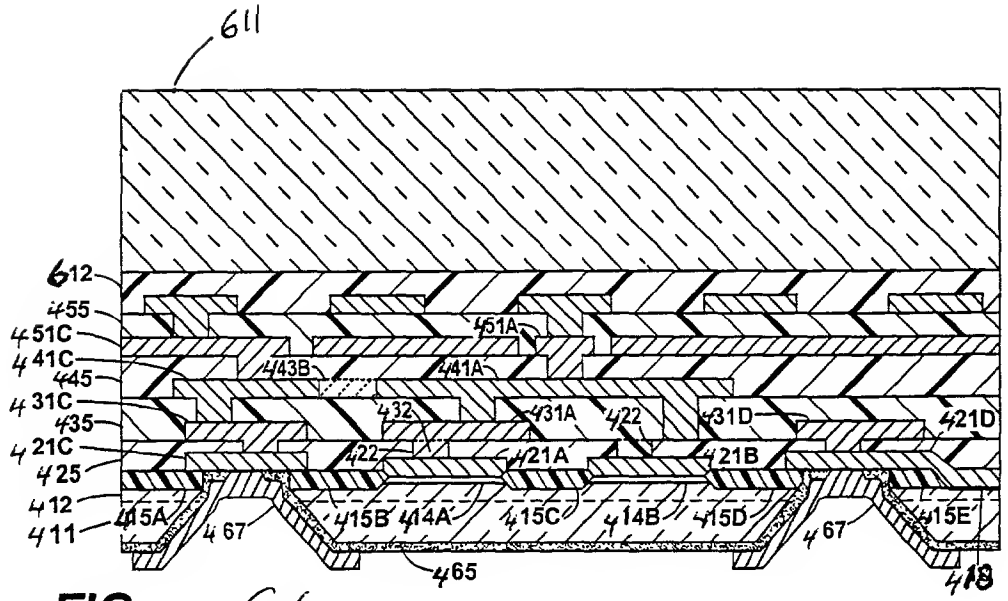
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FIG. 86

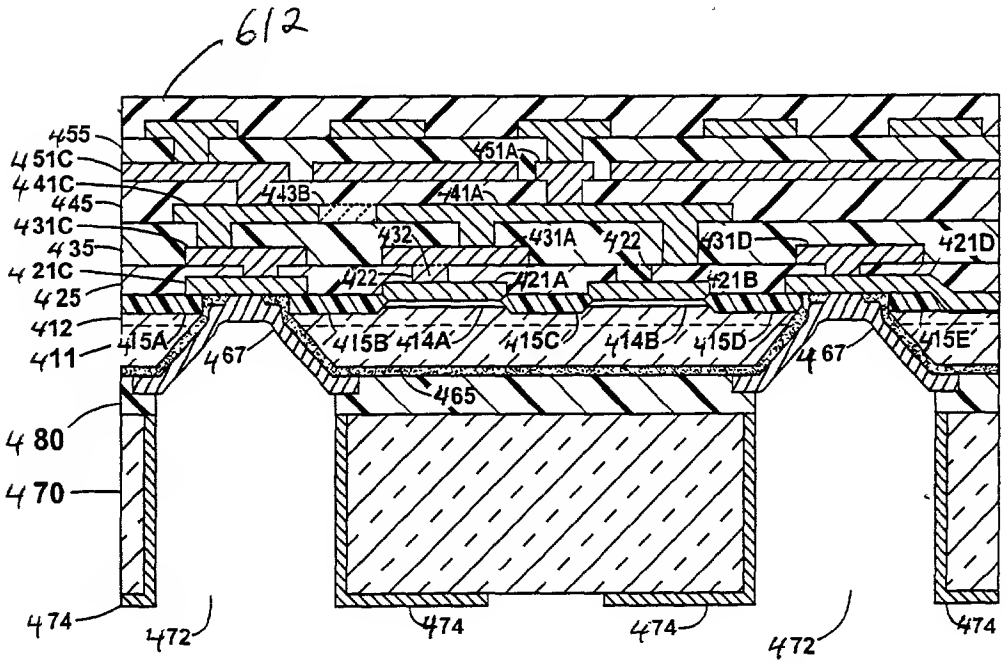
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FIG. 87